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Simulation Study of Improved DDSRF-PLL under Distorted Grid Voltage

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Abstract—When the grid voltage is distorted and harmonic and DC components are mixed, the phase locking accuracy of decoupled double synchronous reference frame for phase-locked loop (DDSRF-PLL) will be greatly reduced. This paper proposes an improved DDSRF-PLL(IDDSRF-PLL) structure based on Frequency Adaptive Sliding Discrete Fourier Transform (FASDFT) filtering. A cascade SDFT structure is adopted for FASDFT filtering. The SDFT with fixed sliding window width at the front stage extracts the fundamental wave signal of power grid voltage to eliminate the influence of harmonics and DC components. The latter SDFT detects the sliding window width of power grid frequency update in real time through a nonlinear tracking differentiator (TD) to suppress spectrum leakage. Then DDSRFT-PLL is used to separate the positive and negative sequence of the fundamental signal and lock the phase. Finally, the simulation results in Matlab/Simulink verify the correctness and effectiveness of the proposed method.

1. Introduction

With the continuous development of distributed new energy generation, the proportion of distributed new energy generation in low-voltage distribution networks has increased significantly. The distribution network shows the characteristics of nonlinear and low damping, which leads to the problems of grid voltage distortion, DC voltage offset, frequency mutation, etc. Therefore, the phase-locked loop is required to maintain the precision of phase-locked under such conditions to ensure the synchronous operation of the grid-connected inverter and power grid.

In [1], scholars studied and analyzed the single synchronous reference frame for phase locked loop. This method has a good phase-locked effect under the ideal working condition of the power grid voltage, but the phase-locked effect is not ideal when the power grid voltage has a three-phase imbalance and contains multiple harmonics. In [2], researchers proposed double second-order generalized integrator PLL. When the distortion of the power grid is low, the phase can be locked quickly and effectively. However, in complex power grids with DC bias and multiple harmonics, the extracted synchronous signal will fluctuate greatly. In [3], researchers use DDSRF-PLL to eliminate the influence of negative sequence voltage components by decoupling module but they didn't consider the influence of harmonic and DC voltage offset on phase locking accuracy.

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2. Operating Principle of DDSRF-PLL

When three-phase unbalance exists in the grid voltage, three-phase voltage U_s is the sum of the positive sequence component U_s^+ and negative sequence component U_s^-.

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = U_s^+ \begin{bmatrix} \sin(\omega t) \\ \sin\left(\omega t - \frac{2}{3}\pi\right) \\ \sin\left(\omega t + \frac{2}{3}\pi\right) \end{bmatrix} + U_s^- \begin{bmatrix} \sin(\omega t + \varphi) \\ \sin\left(\omega t + \varphi + \frac{2}{3}\pi\right) \\ \sin\left(\omega t + \varphi - \frac{2}{3}\pi\right) \end{bmatrix} \tag{1}$$

Where U_s^+ and U_s^- are positive sequence and negative sequence fundamental voltage amplitudes respectively, and φ is the initial phase of negative sequence fundamental voltage.

Converting U_s to the positive order *d,q* coordinate system to obtain:

$$\begin{bmatrix} u_d^+ \\ u_q^+ \end{bmatrix} = U_s^+ \begin{bmatrix} \cos(\omega t - \theta) \\ \sin(\omega t - \theta) \end{bmatrix} + U_s^- \begin{bmatrix} -\cos(\omega t + \varphi + \theta) \\ \sin(\omega t + \varphi + \theta) \end{bmatrix} \tag{2}$$

Where θ is the phase obtained by phase locking.

Converting U_s to the negative order *d,q* coordinate system to obtain:

$$\begin{bmatrix} u_d^- \\ u_q^- \end{bmatrix} = U_s^+ \begin{bmatrix} -\cos(\omega t + \theta) \\ \sin(\omega t + \theta) \end{bmatrix} + U_s^- \begin{bmatrix} \cos(\omega t + \varphi - \theta) \\ \sin(\omega t + \varphi - \theta) \end{bmatrix} \tag{3}$$

Let $\gamma = \omega t - \theta \approx 0$, $\tilde{u}_d^+ = U_s^+ \cos\gamma$, $\tilde{u}_q^+ = U_s^+ \sin\gamma$, $\tilde{u}_d^- = U_s^- \cos\varphi$, $\tilde{u}_q^- = U_s^- \sin\varphi$, by synthesizing Formula (1), we can get:

$$\begin{cases} \begin{bmatrix} u_d^+ \\ u_q^+ \end{bmatrix} \approx \begin{bmatrix} \tilde{u}_d^+ \\ \tilde{u}_q^+ \end{bmatrix} + \tilde{u}_d^- \begin{bmatrix} -\cos(2\omega t) \\ \sin(2\omega t) \end{bmatrix} + \tilde{u}_q^- \begin{bmatrix} \sin(2\omega t) \\ \cos(2\omega t) \end{bmatrix} \\ \begin{bmatrix} u_d^- \\ u_q^- \end{bmatrix} \approx \begin{bmatrix} \tilde{u}_d^- \\ \tilde{u}_q^- \end{bmatrix} + \tilde{u}_d^+ \begin{bmatrix} -\cos(2\omega t) \\ \sin(2\omega t) \end{bmatrix} + \tilde{u}_q^+ \begin{bmatrix} \sin(2\omega t) \\ \cos(2\omega t) \end{bmatrix} \end{cases} \tag{4}$$

According to Formula (1), the positive *d,q* coordinate axis is superimposed with the second harmonic component generated by the direct flow coupling on the negative *d,q* coordinate axis; the negative sequence *d,q* axes are superimposed with the double frequency components generated by the direct flow coupling on the positive sequence *d,q* axes.

Therefore, the decoupling can be completed according to Formula 1, so that the DC component of positive and negative sequence voltage can be obtained to realize phase locking. Its schematic diagram is shown in Figure 1.

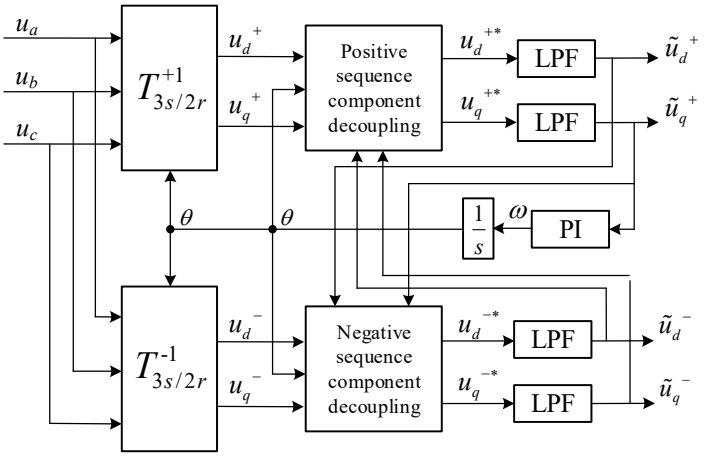


Fig 1 Schematic diagram of DDSRF-PLL

3. Design of FASDFT Filter

The Z-domain transfer function of SDFT[4] is:

$$G_\alpha(z)=\frac{v_\alpha(z)}{v_i(z)}=\frac{1}{N}\left[\frac{1-z^{-N}}{1-e^{j\frac{2\pi}{N}}z^{-1}}+\frac{1-z^{-N}}{1-e^{-j\frac{2\pi}{N}}z^{-1}}\right] \tag{5}$$

Formula (5) Zero pole distribution (N=16) is shown in Figure 2. Its zero points are uniformly distributed on the unit circle and there is zero pole cancellation at the fundamental frequency, the SDFT gain at the fundamental frequency is 0 dB, and the amplitude gain attenuation at other integral times of harmonic frequency is $-\infty$. Therefore, SDFT can completely filter out multiple harmonics and DC offset components under a distorted power grid.

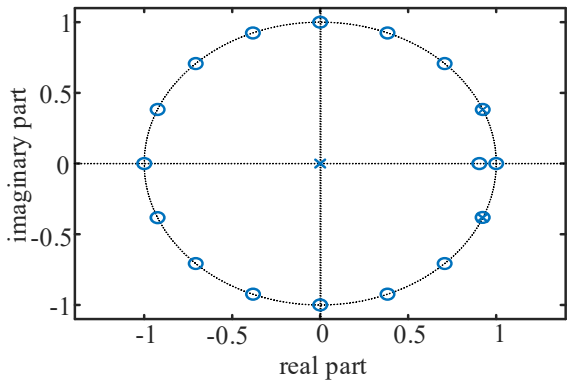


Fig 2 SDFT zero pole distribution map

According to the literature [5], when the grid voltage frequency changes and the SDFT sampling frequency is not N — the times of the fundamental frequency, the system will be unable to accurately extract the fundamental component of the grid voltage, and the harmonic and DC components cannot be eliminated.

To solve this problem, the front stage uses a fixed sliding window width SDFT to estimate the fundamental signal frequency through TD, and the rear stage realizes a variable sliding window width SDFT structure according to the real-time measured frequency value, as shown in Figure 3.

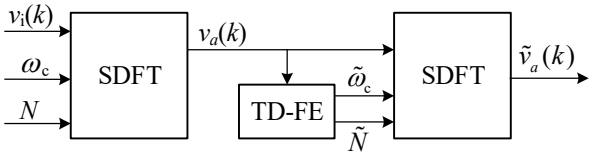


Fig 3 Structure diagram of FASDFT

In Figure 3, the fundamental signal $v_\alpha(k)$ of the input grid voltage sampling value $v_i(k)$ is extracted. $\tilde{N}$ is the number of periodic samples updated by the subsequent level, $\tilde{V}_\alpha(k)$ is the fundamental wave signal output by the subsequent stage, and $\tilde{\omega}_c$ is the real-time frequency estimated by the differentiator.

TD is as shown in Formula (6), using the second-order fastest switching system to track the input signal $v_\alpha(k)$ to obtain $r_1(k)$ and extract the approximate differential signal $r_2(k)$.

$$\begin{cases} r_1(k+1) = r_1(k) + hr_2(k) \\ r_2(k+1) = r_2(k) + h\,\mathrm{fst}(r_1(k) - v_\alpha(k), r_2(k), \delta, h) \end{cases} \tag{6}$$

Where h is the sampling period, δ is the parameter that determines the tracking speed, and fst(·)function is the fastest control comprehensive function, described as follows:

$$\mathrm{fst}(x_1, x_2, \delta, h) \begin{cases} -\delta\,\mathrm{sgn}(a) & |a| > d \\ -\delta\dfrac{a}{d} & |a| \le d \end{cases}, a = \begin{cases} x_2 + \dfrac{a_0 - d}{2}\mathrm{sgn}(y) & |y| > d_0 \\ x_2 + y/h & |y| \le d_0 \end{cases} \tag{7}$$

Where $d = \delta h$； $d_0 = hd$； $y = x_1 + hx_2$； $a_0 = \sqrt{d^2 + 8\delta|y|}$.

Assuming that the fundamental component of the grid voltage is $v_\alpha(k) = r_1(k) = a\sin(\omega_c t)$, the differential signal $r_2(k)$ is obtained by using Equation (5):

$$r_2(k) = a\omega_c \cos(\omega_c t) \tag{8}$$

So we can get:

$$\frac{\int_0^t (r_2(k))^2 \,\mathrm{d}\tau}{\int_0^t (r_1(k))^2 \,\mathrm{d}\tau} = \frac{a^2\omega_c^2 \int_0^t \cos^2(\omega_c\tau)\mathrm{d}\tau}{a^2 \int_0^t \sin^2(\omega_c\tau)\mathrm{d}\tau} = \omega_c^2 \frac{\int_0^t \cos^2(\omega_c\tau)\mathrm{d}\tau}{\int_0^t \sin^2(\omega_c\tau)\mathrm{d}\tau} \tag{9}$$

because

$$\lim_{t\to\infty} \int_0^t \cos^2(\omega_c\tau)\mathrm{d}\tau \Big/ \int_0^t \sin^2(\omega_c\tau)\mathrm{d}\tau = 1 \tag{10}$$

therefore

$$\tilde{\omega}_c \approx \sqrt{\lim_{t\to\infty} \int_0^t (r_2(k))^2 \,\mathrm{d}\tau \Big/ \int_0^t (r_1(k))^2 \,\mathrm{d}\tau} \tag{11}$$

This Formula is also effective for noise-polluted signals. The frequency estimation of fundamental signals is shown in Figure 4.

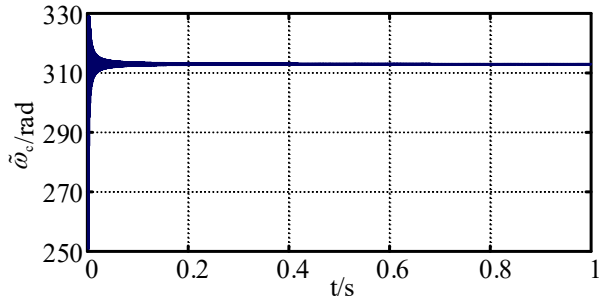


Fig 4 Frequency estimation waveform

The window width of the subsequent SDFT can be changed by changing the number of periodic samples N, and the rounding operation is required. I.e

$$\tilde{N} = round\left(\frac{\pi f_s}{\tilde{\omega}_c}\right) \tag{12}$$

Where f_s is the system sampling frequency.

4. IDDSRF- PLL

The structure diagram of IDDSRF-PLL is shown in Figure 5. Distorted grid voltage can extract its fundamental signal through the FASDFT algorithm, which can avoid the interference of harmonic and DC components of distorted grid voltage on traditional DDSRF-PLL, improve traditional DDSRF-PLL and adapt to a more complex grid environment.

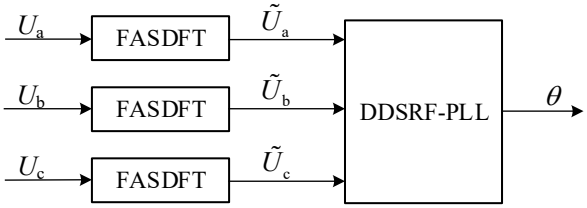


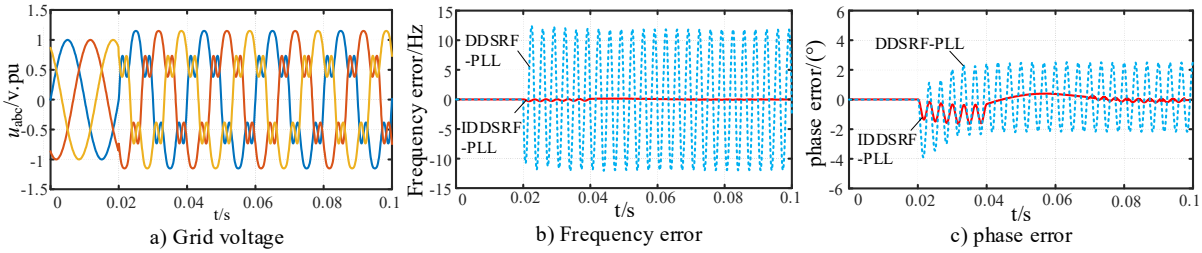
Fig 5 IDDSRF-PLL Structure Diagram

5. Simulation Verification and Performance Analysis

To verify the effectiveness of the IDDSRF-PLL, an improved DDSRF-PLL simulation model is built based on MATLAB/Simulink according to Figure 5 of the structure diagram. In the model, the N value of the preceding SDFT is 128, and the sampling frequency f_s is 12.8 kHz. The simulation is set under three different working conditions and compared with the traditional DDSRF-PLL.

5.1. Condition 1

During the simulation of 0.02 s, the 5th harmonic of 0.3 pu and the 7th harmonic of 0.15 pu injected into the three-phase grid voltage are shown in Figure 6 a), and the frequency error and phase error of the two methods are shown in Figures 6 b) and c).



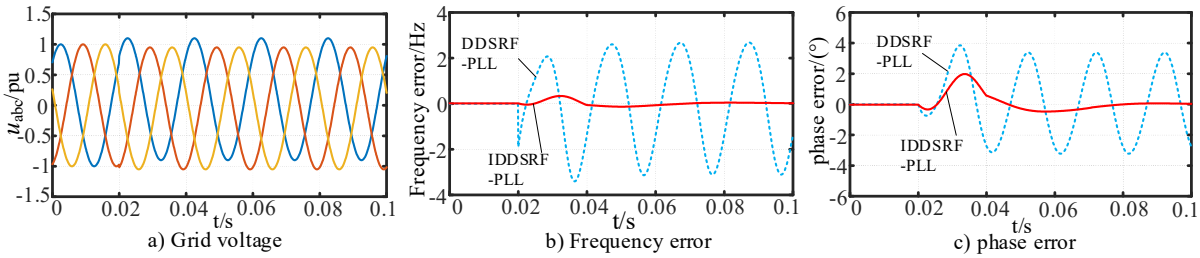
a) Grid voltage b) Frequency error c) phase error

Fig 6 Simulation results of condition 1

The results show that DDSRF-PLL can't achieve accurate phase lock of power grid voltage under harmonic state, and the frequency error and phase error are large. However, IDDSRF-PLL has a small fluctuation in phase error and can quickly realize phase locking. The frequency error is almost unaffected by harmonic injection.

5.2. Condition 2

During the 0.02 s simulation, phasing a voltage superimposes 0.1 pu DC component, then phasing b and c superimpose -0.05 pu DC component. The simulation results are shown in Figure 7.



a) Grid voltage b) Frequency error c) phase error

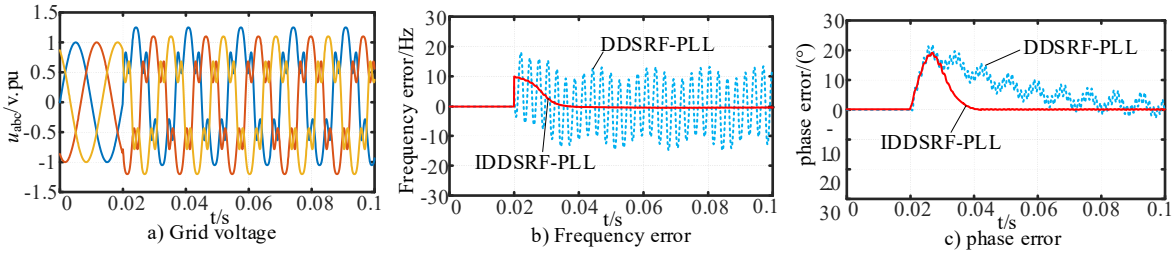
Fig 7 Simulation results of condition 2

It can be seen from Figure 7 that DDSRF-PLL cannot suppress the impact of DC voltage offset, and its phase locking accuracy is seriously affected by DC voltage offset. The output frequency of the improved DDSRF-PLL is almost not affected by the DC voltage offset. After the output phase error oscillates slightly, it quickly returns to zero and tracks the grid voltage phase again.

5.3. Condition 3

Under the premise of harmonic and DC offset under Condition 1 and Condition 2, the power grid frequency suddenly changes from 50 Hz to 60 Hz during the 0.02s simulation, and the simulation results are shown in Figure 8.

The results show that IDDSRF-PLL can suppress the spectrum leakage of SDFT under the working condition of frequency change and eliminate the influence of harmonics and DC bias, then realize fast and accurate phase lock.



a) Grid voltage b) Frequency error c) phase error

Fig 8 Simulation results of condition 3

6. Conclusion

The IDDSRF-PLL based on FASDFT filtering proposed in this paper is essentially a combination of harmonic suppression and DC offset elimination functions based on traditional DDSRF-PLL. Under the condition of severe grid voltage distortion (such as both harmonics and imbalance), it can be used to accurately extract the phase information of the fundamental positive sequence component of the grid voltage from the grid-connected power electronic devices. Then achieving the function of accurate phase locking. The simulation results verify the correctness and feasibility of the algorithm.

References

[1] Tian, G. Z., Wang, S. T., Lin, B. J., & Wang, Z. H. (2010). Design of phase-locked loop based on double synchronous reference frame under unbalanced grid voltage in wind power systems. Electric Drive, 40(7), 53-57.

[2] Ranjan, A., Kewat, S., & Singh, B. (2020). Dsogi-pll with in-loop filter-based solar grid interfaced system for alleviating power quality problems. IEEE Transactions on Industry Applications, PP(99), 1-1.

[3] Rodriguez, P., Pou, J., Bergas, J., Candela, J.I., Burgos, R.P., & Boroyevich, D. (2007). Correction to “decoupled double synchronous reference frame pll for power converters control” [mar 07 584-592]. IEEE Transactions on Power Electronics (3), 22.

[4] Jacobsen, E., & Lyons, R. (2004). An update to the sliding dft. IEEE Signal Processing Magazine, 21(1), 110-111.

[5] Subramanian, C., & Kanagaraj, R. (2015). Rapid tracking of grid variables using prefiltered synchronous reference frame pll. IEEE Transactions on Instrumentation and Measurement, 64(7), 1826-1836.