

PAPER

Low-Complexity Digital Channelizer Design for Software Defined Radio

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SUMMARY In software defined radio systems, a channelizer plays an important role in extracting the desired signals from a wideband signal. Compared to the conventional methods, the proposed scheme provides a solution to design a digital channelizer extracting the multiple subband signals at different center frequencies with low complexity. To do this, this paper formulates the problem as an optimization problem, which minimizes the required multiplications number subject to the constraints of the ripple in the passbands and the stopbands for single channel and combined multiple channels. In addition, a solution to solve the optimization problem is also presented and the corresponding structure is demonstrated. Simulation results show that the proposed scheme requires smaller number of the multiplications than other conventional methods. Moreover, unlike other methods, this structure can process signals with different bandwidths at different center frequencies simultaneously only by changing the status of the corresponding multiplexers without hardware reimplementation.

key words: low-complexity, fast filter bank, digital channelizer, software defined radio

1. Introduction

As demand for wireless communication increases, it is important to modify the radio device to support different wireless radio communication standards without hardware reimplementation. Under this condition, software defined radio (SDR) as a promising technology attracts more and more attention. SDR can process signals related to different standards only by software update without reimplementation of hardware architecture, which provides a flexible and cost-effective solution of resource utilization. In SDR based systems such as cognitive radio, multi-standard wireless receivers and so on, a channelizer is the most computationally intensive and power consuming block and plays an important role in exacting the desired signals from the wideband received signals [1], [2].

A conventional method to implement channelizers is based on the discrete Fourier transform filter bank (DFTFB) in [3], [4]. The modulated perfect reconstruction filter bank (MPRFB) [5] and the cosine modulated filter bank (CMFB) [6], [7] are two types of filter banks, which provide uniform and nonuniform channelization. In [8], [9], a flexible low complexity uniform and nonuniform digital filter banks with high frequency resolution is proposed for multistandard radios. A low-complexity reconfigurable filter bank chan-

nelizer is designed based on coefficient decimation, interpolation and frequency masking techniques in [10]. A new reconfigurable filter bank architecture based on frequency response masking (FRM) for the SDR channelizer is proposed in [11], [12]. In [13], a VDF (variable digital filter) based on the improved coefficient decimation method (ICDM) is proposed, which provides variable lowpass, highpass, bandpass, bandstop and multi-band frequency responses on-the-fly, using the same set of prototype filter coefficients.

Recently, channelizers based on fast filter bank have been reported by exploiting its good properties such as high selectivity, sparse coefficients and so on, and achieved better performance in the context of SDR based systems. In [14], fast filter bank is used to design the channelizer for spectrum sensing in military radio receivers. The total number of multiplications used in the proposed architecture has a complexity reduction over DFTFB, MPRFB and CMFB based methods. In [15], it provided a reconfigurable solution for the variable digital filter with low complexity. However, the above methods were unsuitable for processing the signals with multiple bandwidths at different center frequencies at the same time. In addition, the prototype filter based on fast filter bank is designed under the assumptions that the passband ripples of all subfilters are equal. As a result, it could not control the ripple tolerance and the passband edge frequency of the prototype filter at each stage exactly, which results in that there is potential to reduce the complexity further.

To do this, this paper demonstrates a structure to process radio signals with multiple bandwidths at different center frequencies. In order to satisfy the specifications for different bandwidths with minimum number of multiplications, this paper formulates the problem as an optimization, which controls the ripple in the passband and the stopband when combining adjacent sub-channels. In this manner, the hardware structure is not required to be modified to form different bandwidths only by selecting appropriate sub-channels of the proposed cascaded filter bank simply. For the purpose of applications, a practical method is also provided. Simulation results show that the proposed scheme can achieve multiplications reduction over other solutions and can process multi-standard signals with different bandwidths at the different center frequencies simultaneously.

The rest of this paper is organized as follows. In Sect. 2, fast filter bank is introduced briefly. In the following, a practical structure is proposed and explained in Sect. 3. Section 4 formulates the prototype filters design as an optimization

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problem and the solution is discussed in detail to reduce the complexity of the channelizer while keeping the ripple in the passband and stopband to satisfy the specifications for the different bandwidths. Design process is also discussed in this section. Simulations are used to verify the performance of the proposed scheme in Sect. 5. Section 6 concludes the paper.

2. Review of Cascaded Filter Bank

Fast filter bank was first introduced as a general form of sliding fast Fourier transform (FFT) filter bank in [16]. Specifically, a L -stage analysis fast filter bank can decompose the input signal into N channels in the frequency range from 0 to 2π normalized frequency in radian per sample, where $N = 2^L$ and L is an integer. For the k -th stage, there are 2^L subfilters in this stage, where k ranges from 0 to $L - 1$. For convenience, the m -th subfilter at the k -th stage is abbreviated as the (k, m) subfilter. All the subfilters for the analysis fast filter bank exhibit the similar structure shown in Fig. 1.

A (k, m) subfilter can be modeled as a system with one input and two outputs in Fig. 1, where m is an integer between 0 and $2^k - 1$. The transfer function of the upper path denotes $H_a^{k,m}(z)$, while the transfer function of the lower path is described as $H_c^{k,m}(z)$. Two outputs of the subfilter are complementary with the relationship expressed as follows in Eq. (1).

$$H_a^{k,m}(z) + H_c^{k,m}(z) = 2 \quad (1)$$

At the k -th stage, the transfer function of the upper path, $H_a^{k,m}(z)$, can be obtained by replacing each z in the prototype lowpass halfband filter $H_a^k(z)$ with $W_N^{\tilde{m}} z^{2^{L-k-1}}$, where $\tilde{m}$ is the bit reversed version of m in $L - 1$ bits. In this manner, the transfer function of the m -th subfilter at the k -th stage can be computed in Eq. (2) when the prototype lowpass filter transfer function $H_a^k(z)$ is given.

$$\begin{aligned} H_a^{k,m}(z) &= H_a^k(W_N^{\tilde{m}} z^{2^{L-k-1}}) \\ H_c^{k,m}(z) &= 2 - H_a^k(W_N^{\tilde{m}} z^{2^{L-k-1}}) \\ W_N &= e^{-j2\pi/N} \end{aligned} \quad (2)$$

When the subfilters at each stage for channel n_0 are determined, the transfer function of the channel n_0 in z domain, $H_{n_0}(z)$, can be written with the form in Eq. (3),

$$H_{n_0}(z) = \frac{1}{N} \prod_{k=0,1,\dots,L-1} H_{p_k}^{k,m_k}(z) \quad (3)$$

where ' $\prod$ ' presents the multiplication of the elements. k

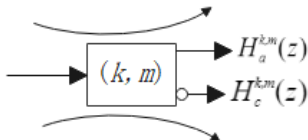


Fig. 1 Structure of the (k, m) subfilter.

represents the stage number ranging from 0 to $L - 1$. m_k is described as the subfilter index of channel n_0 at the k -th stage. p_k indicates the upper path or the lower path. When the channel n_0 includes the upper path of the (k, m_k) subfilter, p_k stands for 'a', that is, the transfer function $H_a^{k,m_k}(z)$, otherwise, the transfer function is the complementary component, $H_c^{k,m_k}(z)$.

3. Proposed Channelizer Structure

Referring to the characteristics in Eqs. (1) and (3), the Eq. (4) can be derived, that is, the output transfer functions of all channels may be summed to a constant, which means that the filter bank is equivalent to an allpass filter in the normalized frequency interval $[0, 2\pi]$ when combining all the outputs. Based on this property, a practical equivalent structure is proposed for the digital channelizer shown in Fig. 2.

$$\sum_{n_0=0}^{N-1} H_{n_0}(z) = \text{constant} \quad (4)$$

In Fig. 2, the proposed structure is composed of the cascaded filter bank structure, multiplexer array composed of the elements marked with $M_0, M_1, \dots, M_{N-1}$ and the summation unit. A multiplexer element has two data input ports marked with ' D_0 ' and ' D_1 ' and one output port (' F ') controlled by the control port (' C '). For the k -th multiplexer element M_k , by setting the control port ' C ' to the value '0' determines that the input data port ' D_0 ' connects to the output port ' F ', otherwise, the input data port ' D_1 ' connects to the output port. All the splitted signals from cascaded filter bank are connected to the input ports ' D_1 ' of the corresponding multiplexer elements, while the input ports ' D_0 ' are connected to the value '0'.

The input signal X decomposes N subbands in the frequency domain when it passes the cascaded filter bank structure. If some decomposed signals are the desired signals in frequency domain, they can be transferred to the summation unit by setting the value '1' to the control port ' C ' in their corresponding connected multiplexer elements. Otherwise, the value '0' can be connected to the summation unit by setting '0' to the control port with the result that the decomposed signals can be removed from the input signal in the frequency domain. In this manner, the digital channelizer can implement arbitrary passband and stopband in the

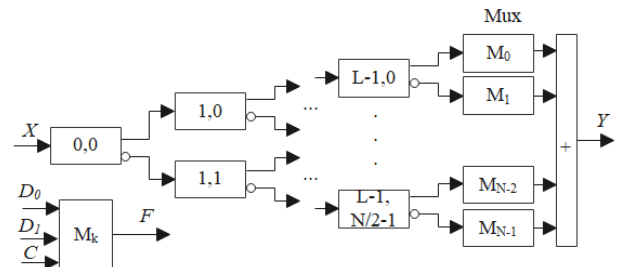


Fig. 2 Equivalent structure of the channelizer.

normalized frequency domain only by changing the status of the control ports of the multiplexer elements in the multiplexer array, which means that the proposed solution can process signals at different center frequencies with different bandwidths for multi-standard signals simultaneously.

In the following, design process will be discussed in detail for the optimal prototype lowpass filter of each stage to meet the constraints with low complexity when combining the desired channel using the proposed structure in Fig. 2.

4. Prototype Filter Optimization and Design Process

The problem to design the digital channelizer of the proposed scheme is formulated as an optimization problem of minimizing the total number of multiplications subject to the constrained ripple in the passband and stopband when combining the adjacent channels. In this manner, it can be achieved by controlling the ripple magnitude tolerance and the passband edge frequency of each subfilter according to the overall specifications, which has not been reported in the literatures. In this section, a method is proposed to obtain the optimal or suboptimal solution to the optimization problem.

4.1 Optimization Problem

It is known that finite impulse response filter(FIR) with odd length and even symmetrical property is valid for different types filters. In this paper, for the sake of simplicity, the impulse response coefficients of the prototype filter for each stage are assumed to be even symmetrical and with odd length. In addition, noncausal halfband prototype filter is further assumed, that is, the transfer function $H_a^k(z)$ at the k -th stage can be constructed with the odd length $2M_k + 1$ in a form in Eq. (5), where $h_a^k(n)$ is the impulse response of $H_a^k(z)$ at time n .

$$H_a^k(z) = \sum_{n=-M_k}^{M_k} h_a^k(n)z^{-n} \quad h_a^k(n) = h_a^k(-n) \quad (5)$$

For a halfband filter, the required number of multiplications is about one-quarter of its length. In order to decrease the number of multiplications, the prototype lowpass filters for all stages are treated as the halfband filters. Therefore, the required number of multiplications for the subfilters at the k -th stage is $\lfloor (M_k + 1)/2 \rfloor$, where $\lfloor x \rfloor$ represents the maximum integer no more than x . Accordingly, the total number of multiplications of the proposed scheme, M , can be calculated with required multiplications in all stages and rewritten with a form in Eq. (6).

$$M = \sum_{k=0}^{L-1} 2^k \cdot \lfloor (M_k + 1)/2 \rfloor \quad (6)$$

The channel number of the cascaded filter bank N depends on the resolution of the system R evaluated in Eq. (7), where f_s is the sampling rate, $\log_2(x)$ represents the logarithm of the base 2 and $\lceil \cdot \rceil$ is the smallest integer greater than a certain number.

$$N = 2^{\lceil \log_2(f_s/R) \rceil} \quad (7)$$

The frequency response of the 0-th channel can be regarded as the indicator of constraints for the single channel due to that the frequency responses of other channels are the shifted versions of that of the 0-th channel. For a wider bandwidth formed by combining some adjacent channels, the frequency response changes in comparison with that of the single channel. In order to make the frequency response for the different wider bandwidth acceptable, the frequency response of three adjacent channels are chosen to be as a constraint condition for the optimal design of the prototype lowpass filter.

In general, the specifications for a FIR filter are the passband edge frequency, the peak passband ripple, the stopband edge frequency and the peak stopband ripple. Similarly, in this paper, the prototype lowpass filter of the channels are listed as follows, in normalized frequency domain ranging from 0 to 2π .

Passband edge frequency: ω_p ; Peak passband ripple: δ_p ;
Stopband edge frequency: ω_s ; Peak stopband ripple: δ_s .

As above stated, to design the channelizers with as small number of multiplications as possible subject to the constraints, it can be treated as an optimization problem defined in Eq. (8), where $H_0(e^{j\omega})$ can be derived from Eqs. (2) and (3) by replacing z with $e^{j\omega}$ and $H_{comb}(e^{j\omega})$ is the frequency response of three adjacent channels, that is, channels 0, 1 and $N - 1$ expressed in Eq. (9) considering the symmetrical characteristics of the combined wider bandwidth.

$$\begin{aligned} \min \quad & M \\ \text{s.t.} \quad & |H_0(e^{j\omega}) - 1| \leq \delta_p \quad |\omega| \leq \frac{\omega_p}{N/2} \\ & |H_0(e^{j\omega})| \leq \delta_s \quad \frac{\omega_s}{N/2} \leq |\omega| \leq \pi \end{aligned} \quad (8)$$

$$\begin{aligned} & |H_{comb}(e^{j\omega}) - 1| \leq \delta_p \quad |\omega| \leq \frac{\pi}{N} + \frac{\omega_p}{N/2} \\ & |H_{comb}(e^{j\omega})| \leq \delta_s \quad \frac{\pi}{N} + \frac{\omega_s}{N/2} \leq |\omega| \leq \pi \\ & H_{comb}(e^{j\omega}) = H_0(e^{j\omega}) + H_1(e^{j\omega}) + H_{N-1}(e^{j\omega}) \end{aligned} \quad (9)$$

4.2 Optimization Solution

In this subsection, an optimization solution is proposed to solve the problem in Eq. (8). In order to implement the channelizer with minimum number of multiplications, a halfband filter method is utilized to design the prototype filter at each stage. In this case, the specifications for the prototype filter at the k -th stage can be reduced to the passband edge frequency ω_p^k and the passband ripple δ_p^k , because the stopband edge frequency ω_s^k and the stopband ripple δ_s^k can be determined with ω_p^k and δ_p^k in (10).

$$\omega_s^k = \pi - \omega_p^k \quad \delta_s^k = \delta_p^k \quad (10)$$

At the k -th stage of the cascaded filter bank, the length of the prototype filter, $2M_k + 1$, can be evaluated by (11).

$$2M_k + 1 \approx \frac{-20\pi \cdot \log_{10}(\delta_p^k \cdot \delta_s^k) - 13}{14.6(\omega_s^k - \omega_p^k)} + 1 \quad (11)$$

Substituting (10) in (11), it follows:

$$2M_k + 1 \approx \frac{-40\pi \cdot \log_{10}(\delta_p^k) - 13}{14.6(\pi - 2\omega_p^k)} + 1 \quad (12)$$

From Eqs. (10), (11) and (12), it can be deduced that to minimize the total number of multiplications M can be achieved by minimizing the length of the prototype filter $2M_k + 1$ for each stage, which is equivalent to make the passband edge frequency ω_p^k as small as possible and the ripple in the passband δ_p^k as large as possible for the prototype filter under the constraints in (8).

For the purpose of obtaining minimum number of multiplications, it is hard to choose appropriate specifications to design prototype lowpass filters to satisfy the constraints directly. To do this, an iterative method based on relaxing specifications in reverser order is proposed, that is, the parameters are adjusted for the prototype lowpass filter at the k -th stage from the last stage ($k = L - 1$) down to the first stage ($k = 0$).

Some constants should be predefined for adjusting specifications of the prototype lowpass filters. The parameter $\Delta\delta_p$ is defined for adjusting the ripple in the passband and $\Delta\omega_p$ for adjusting the passband edge frequency.

The proposed algorithm is illustrated as follows.

Step 1: Initialization of the specifications: Choosing ω_p^k and δ_p^k to meet the requirements defined in Eq. (8), where k ranges from 0 to $L - 1$. Assigning current stage index for adjusting design parameters, k_c , to the last stage $L - 1$.

Step 2: According to the specifications ω_p^k and δ_p^k , the impulse response coefficients $h_a^k(n)$ and the length of the prototype filter $2M_k + 1$ can be computed by one of finite filter design methods such as halfband method.

Step 3: Calculating the frequency response of the 0-th channel $H_0(e^{j\omega})$ and the combined wider channels $H_{comb}(e^{j\omega})$ according to the Eqs. (2), (3) and (9). If $H_0(e^{j\omega})$ and $H_{comb}(e^{j\omega})$ meet the constraints in Eq. (8), the specifications at the k_c -th stage can be adjusted with Eq. (13), and procedure performs Step 2. Otherwise, the procedure performs Step 4.

$$\omega_p^{k_c} = \omega_p^{k_c} - \Delta\omega_p \quad \delta_p^{k_c} = \delta_p^{k_c} + \Delta\delta_p \quad (13)$$

Step 4: Restoring the invalid specifications with Eq. (14). In the following, the current stage index k_c is updated with the next stage index by setting $k_c = k_c - 1$. If k_c is less than zero, the procedure completes. Otherwise, the procedure performs Step 2.

$$\omega_p^{k_c} = \omega_p^{k_c} + \Delta\omega_p \quad \delta_p^{k_c} = \delta_p^{k_c} - \Delta\delta_p \quad (14)$$

With the proposed solution, the optimal or suboptimal specifications of the prototype filters, ω_p^k and δ_p^k , are determined, then the impulse response coefficients $h_a^k(n)$ and the length of the prototype $2M_k + 1$ can be calculated. As a result, the total number of multiplications can be also computed using Eq. (6).

4.3 Design Process

When the prototype lowpass filter completes for each stage

in Sect. 4.2, design process is discussed. In this subsection, a generalized case is considered. It is assumed that there are some signals within several passbands in frequency domain with the sampling rate f_s and the resolution is R . The number of multi-standard signals is P within the frequency range $[f_l(p), f_h(p)]$ for the p -th signal, where p ranges from 0 to $P - 1$. $f_l(p)$ represents the low frequency of the p -th signal and $f_h(p)$ is the symbol for the high frequency of the p -th signal.

Using Eq. (7), the channel number of the proposed structure, N , can be evaluated. Then, the real resolution of the system R_1 can be computed with the expression in Eq. (15).

$$R_1 = \frac{f_s}{N} \quad (15)$$

With the help of real resolution R_1 , normalized indices set for the p -th signal, $[n_l(p), n_h(p)]$, is calculated using Eq. (16), where ' $\lfloor \cdot \rfloor$ ' indicates the maximum integer not more than a number. This set $[n_l(p), n_h(p)]$ means the continuous integer from $n_l(p)$ to $n_h(p)$ and this set is also regarded as the desired channel number set.

$$n_l(p) = \left\lfloor \frac{f_l(p)}{R_1} \right\rfloor \quad n_h(p) = \left\lfloor \frac{f_h(p)}{R_1} \right\rfloor \quad (16)$$

When the corresponding indices set for the p -th signal are determined, the control port status of the elements in the multiplexer array depicted in Fig. 2 can be set accordingly, that is, the indices are accordance with the status of the multiplexers.

To explain clearly, a control vector $\mathbf{C}$ is defined as a collection of the control port status of the multiplexer $M_0, M_1, \dots, M_{N-1}$ with the elements $c_0, c_1, \dots, c_{N-1}$, that is, the control vector $\mathbf{C} = \{c_0, c_1, \dots, c_{N-1}\}$, where the element in the vector c_k indicates the control port status of the multiplexer M_k with the value 0 or 1.

When the channel number n_0 belongs to the channel vector $[n_l(p), n_h(p)]$, the index of the corresponding multiplexer is $M_{\tilde{n}_0}$, where $\tilde{n}_0$ is the bit reversed version of n_0 in $L - 1$ bits described in Sect. 2. With the relationship the multiplexer index and the channel number, the element $c_{\tilde{n}_0}$ in the control vector $\mathbf{C}$ should be set to the value 1.

When all control ports of the multiplexers are set proper status, the transfer function of the system, $H(z)$, can be determined with the form in Eq. (17). With this structure, the proposed structure can process signals at different center frequencies with different bandwidth. The multiple subbands will be adjusted only by changing the control vector $\mathbf{C}$ and the corresponding the control ports status of the multiplexers without hardware reimplementation.

$$H(z) = \sum_{p=0}^{P-1} \sum_{n_0 \in [n_l(p), n_h(p)]} H_{n_0}(z) \quad (17)$$

5. Simulation and Analysis

In this section, multi-standard signals processing is used as

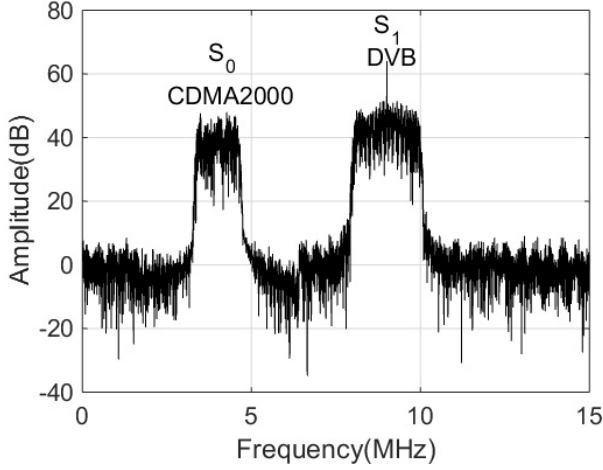


Fig. 3 Spectrum of the input signal.

an example to verify the performance of the proposed scheme and evaluate the complexity.

The input test signal is composed of two multi-standard signals. One signal, S_0 , is code division multiple access 2000 (CDMA2000) signal with 1 MHz bandwidth at the center frequency 4 MHz. The other signal, S_1 , is digital video broadcasting (DVB) signal located at the center frequency 9 MHz with 2 MHz bandwidth. The spectrum of the input signal analyzed by FFT is illustrated in Fig. 3, where it can be observed that the signal in the passband is about 40 dB higher than the noise in the stopband. The sampling rate of the channelizer f_s is set to be 15 MHz and the allowable desired resolution of frequency is set to be 0.25 MHz in the simulation.

Based on the sampling rate, allowable desired resolution of frequency and Eq. (7), the channel number of the filter bank N is evaluated by $N \approx f_s/0.25 = 60$. Because channel number N is an integer of power 2, it can be chosen $N = 64$ in the simulation. The overall specifications are listed as follows: the passband edge frequency $\omega_p = 0.37\pi/N$, the passband ripple $\delta_p = 0.08$ dB (0.0093), the stopband edge frequency $\omega_s = 0.63\pi/N$ and the stopband ripple $\delta_s = -50$ dB (0.0032).

In the following, the prototype lowpass filter for each stage can be designed with the optimization solution in Sect. 4. The number of stages L can be calculated with $L = \log_2(N) = 6$. According to the specifications, the proposed scheme performs with initial values of the specifications for the prototype filter of cascaded filter bank and the adjusting parameters, that is, $\omega_p^k = 0.2\pi$, $\delta_p^k = 0.0162$ (0.1400 dB) for $k = 0, 1, \dots, L-1$. The predefined parameters for relaxing the specifications, $\Delta\delta_p$ is set to be 0.00001 and $\Delta\omega_p$ is set to be 0.00001 π .

With the proposed algorithm, the impulse response coefficients of the prototype lowpass filter for each stage are determined, and the nonzero coefficients are listed in Table 1.

The magnitude frequency response of the 0-th channel is shown in Fig. 4, from which it can be seen that the magnitude frequency response of the 0-th channel can meet

Table 1 Impulse response of prototype filters for $h_a^k(n)$.

n	$h_a^0(n)$	$h_a^1(n)$	$h_a^2(n)$	$h_a^3(n)$	$h_a^4(n)$	$h_a^5(n)$
0	1.000	1.0000	1.0000	1.0000	1.0000	1.0000
± 1	0.6255	0.6096	0.5836	0.5005	0.5003	0.5001
± 3	-0.1806	-0.1411	-0.0896			
± 5	0.0801	0.0365				
± 7	-0.0347					
± 9	0.0129					

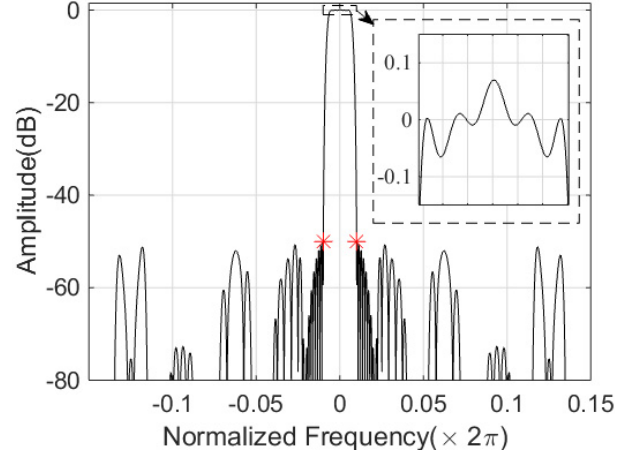


Fig. 4 Magnitude frequency response of the 0-th channel.

the requirements of the overall specifications.

From Table 1, the number of multiplications required by the channelizer designed with the proposed scheme M can be determined with (18) according to (6), that is, $M = 75$.

$$M = 5 \times 1 + 3 \times 2 + 2 \times 4 + 1 \times 8 + 1 \times 16 + 1 \times 32 = 75 \quad (18)$$

To evaluate the performance of the proposed solution, the number of multiplications of the proposed method is compared with DFTFB, MPRB, CMFB and ICDM based VDF. For the reference methods, the order of the prototype filter can be computed with Eq. (19),

$$N_f = \left\lceil -\frac{4\log_{10}(10\delta_p\delta_s)}{3(f_s - f_p)} - 1 \right\rceil + \left\lceil \frac{4\log_{10}M}{3(f_s - f_p)} \right\rceil \quad (19)$$

where N_f is the order of the prototype filter, f_p and f_s are the normalized passband and stopband cutoff frequencies of the prototype filter corresponds to half of the sampling frequency and determined with the desired specifications ω_p and ω_s using $f_p = \omega_p/\pi$ and $f_s = \omega_s/\pi$, M is the maximum possible decimation factor without aliasing.

For DFTFB, MPRB and CMFB, the order of the prototype filter can be computed by the first term on the right-hand side of Eq. (19), that is, N_f equals to 408 with the specifications. Considering the symmetry of the impulse response coefficients of the prototype filter, the required number of multiplications is about half of the order of the prototype filter and the number of multiplications is 204 in this case. In addition, DFT is required by the three methods and the multiplications number is related to the channel number N referring to Table 2.

Table 2 Comparison of multiplication number.

Method	DFTFB	MPRB	CMFB	VDF	Prop.
Filter Mult.	204	$2 \times 204 = 408$	204	204	75
DFT Mult.	$N \log_2 N = 384$	$2 \times N \log_2 N = 768$	$N^2 = 4096$	-	-
Tot. Mult.	588	972	4300	204	75

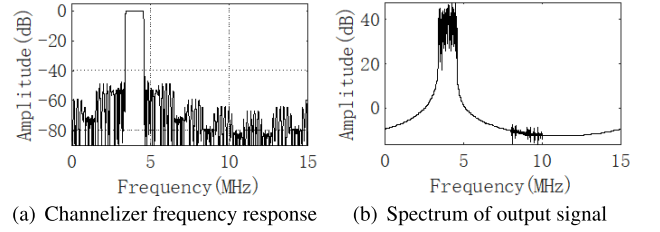
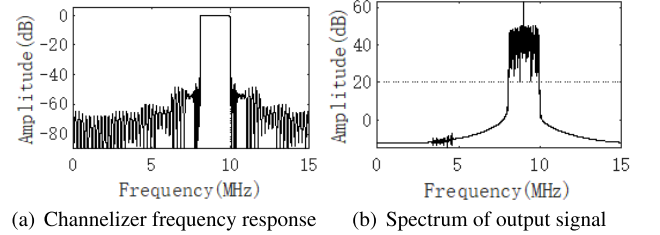
For ICDM based VDF, the number of the prototype filter can be evaluated with Eq. (19). The value of the second term on the right-hand of Eq. (19) varies depending on the decimation factor M . Therefore, the minimum possible order for ICDM based VDF is determined by first term in the equation. Consequently, the required number of multiplications is about 204 without DFT operation shown as in Table 2. It can be observed that the proposed cascaded filter bank requires less number of multiplications.

According to the center frequencies and passband bandwidths of the desired channelizer, the corresponding channel indices and the channel vector of the proposed scheme can be determined according to Eq. (16). For the signal S_0 , the center frequency is 4 MHz with 1 MHz bandwidth. It can be deduced that the frequency of signal S_0 is from 3.5 MHz to 4.5 MHz. Using Eq. (16), the channel vector can be calculated. In specifically, the desired channel number ranges from 14 to 20. The bit reversed versions in $L - 1$ bits of the desired channel vector is 14, 30, 1, 17, 9, 25, 5. According to the channel vector, in the control vector C , the elements $c_{14}, c_{30}, c_1, c_{17}, c_9, c_{25}, c_5$ are set to the value 1 and other elements in the vector C are kept zeros. In accordance with the vector C , the control ports of $M_{14}, M_{30}, M_1, M_{17}, M_9, M_{25}, M_5$ in the multiplexer array are set to the value 1 and the control ports of other multiplexers in the array are set to the value 0.

Similarly, for the signal S_1 , the desired combining channel vector is {29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39}. The corresponding bit reversed versions in $L - 1$ bits are {23, 15, 31, 1, 33, 17, 49, 9, 41, 25, 57}. Using the bit reversed version, the control ports of the corresponding multiplexers can be set to be 1 similar to the operation for the signal S_0 .

When all the control ports of the multiplexers are set, the proposed structure can extract the different signal at different center frequencies with different bandwidths at the same time. In the simulation, the magnitude frequency responses of the channelizer are depicted in Figs. 5(a) and 6(a) according to Eq. (17). The input signal passes through the channelizer determined by the sets and forms two desired extracted output signals with the spectrums in Figs. 5(b) and 6(b). From Figs. 5 and 6, it can be seen that the desired signals can be exacted from the wide bandwidth input signal. In addition, the attenuation in the stopband of the extracted output signals is about -50 dB higher than that of the input signal analyzed with FFT in Fig. 3, which verifies the property of high attenuation of the filter bank when compared with FFT.

The simulation results show that the proposed scheme can exact desired signals from a wideband received signal at different center frequencies with different bandwidths si-

**Fig. 5** Performance of the channelized signal S_0 .**Fig. 6** Performance of the channelized signal S_1 .

multaneously and be applicable for the design of the digital channelizer in the context of SDR system with low complexity.

6. Conclusion

Digital channelizers are used to extract the desired signals from a wideband received signal in SDR system. In this paper, a cascaded filter bank based structure is proposed consisting of the cascaded bank, multiplexer array and the summation unit. The change of the specifications such as bandwidths and center frequencies can be achieved by setting the appropriate control port of the corresponding multiplexer in the multiplexer array simply. In order to make the ripples in the passband and the stopband satisfy the specification when combining the adjacent sub-channels are combined and different bandwidths are formed, this paper formulates the problem an optimization problem, which minimizes the required number of multiplications subject to the ripple in the passband and the stopband for the single channel and the combined desired channels. To obtain the suboptimal resolution, an iterative method is developed by relaxing the specifications in the reversed order of the stage. Simulations verify the performance of that the proposed scheme can extract the desired signals from the input signal with low complexity compared to the conventional methods such as DFTFB, MPRB, CMFB and ICDM based VDF. In addition, the proposed scheme can process signals at different center frequencies with different bandwidths simultaneously only by changing the status of corresponding multiplexers with the same hardware structure without recalculating the impulse response coefficients of the filter banks.

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