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Hydrogen-Terminated Diamond Field-Effect Transistors with Ultrahigh On/Off Ratio Using an Al2O3/HfO2 Stacked Passivation Layer

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Abstract

Diamond-based devices with high on/off ratio are promising candidates for power and sensors applications at high temperatures. However, the limited on/off ratio caused by relatively high leakage currents still remains to be a problem. Herein, we present hydrogen-terminated diamond metal–insulator–semiconductor field-effect transistors with a 40-/100-nm aluminum oxide/hafnium dioxide stacked passivation layer to reduce leakage currents. Due to the stacked passivation layer, the fringing capacitances were introduced and the electric field at the drain edge of the gate was reduced. Encouragingly, the drain and gate leakage currents were reduced to the order of 10^{-9} mA/mm under off-state conditions at room temperature. Consequently, an on/off ratio of ~1×10^{11} was achieved, which is the highest value among the previously reported diamond-based devices. Moreover, a record on/off ratio of ~5×10^{9} was obtained even at 200°C. Results of this work can pave the way for diamond-based devices in high-temperature power or sensors applications.

Full Text

With the advancements in the field of automobile and aerospace, there is a demand for the power electronics and sensors that can reliably operate at high temperature (>200 °C). Generally, silicon (Si)-based bulk complementary metal–oxide–semiconductor (CMOS) is not reliable when the temperature exceed 125°C due to a prominent increased leakage current (thermal runaway).[1,2] Simultaneously, a high output current under on-state conditions is also required. Therefore, alternative field-effect transistors (FETs) with a high current on/off ratio at high temperature are desired for low power consumption. A few methods have been proposed to increase the on/off ratio; reducing gate leakage current ($I_{G_leakage}$) and drain leakage current ($I_{D_leakage}$) is one way of increasing the ratio. For example, inserting an insulator layer under the gate metal can increase the potential barrier and decrease $I_{G_leakage}$ eventually, or using a high-k gate dielectric to enhance the gate control ability can reduce $I_{D_leakage}$. Another method is to achieve low on-resistance (R_{ON}) to increase output current; for example, increasing carrier mobility and concentration as well as reducing trapping effects can increase output current.

Wide-bandgap semiconductor FETs can reduce the drift region length and increase the doping concentration to increase the output current. Furthermore, it can withstand high voltages and temperatures for achieving a low leakage current; hence, they can easily achieve a high on/off ratio and are more suitable for high-temperature operations compared with Si. Recently, wide bandgap semiconductors, such as gallium nitride (GaN) and silicon carbide (SiC), have been widely used in radio frequency and power applications. To further achieve high reliability and good performance in high temperature applications, ultrawide bandgap semiconductors, such as diamond and gallium oxide (Ga_2O_3), are gaining attention recently. Compared with Ga_2O_3, due to the advantages of a high breakdown electric field (>10 MV/cm), excellent thermal conductivity (>22 $W \cdot cm^{-1} \cdot K^{-1}$), and high carrier mobility (3800 $cm^2 \cdot V^{-1} \cdot s^{-1}$ for hole, 4500 $cm^2 \cdot V^{-1} \cdot s^{-1}$ for electron)[3], diamond has more potential for applications in extreme environments, e.g., high temperature. Interestingly, even without intentional

doping, hydrogen-terminated (C–H) diamond exhibits a subsurface two-dimensional hole gas (2DHG) layer via surface adsorbates[4,5]. However, the 2DHG can be affected by the surrounding environment, inducing instability in the conductivity of the C–H diamonds[6,7]. Therefore, various dielectrics have been used as gate dielectric layer and passivation layers to enhance the stability of the C–H diamond, such as aluminum oxide (Al_2O_3)[8], hafnium dioxide (HfO_2)[9], molybdenum oxide (MoO_3)[10], vanadium oxide (V_2O_5)[11], silicon nitride (SiN_x)[12], and hexagonal boron nitride (h-BN)[13]. Among them, C–H diamond metal–insulator–semiconductor FETs (MISFETs) with an Al_2O_3 dielectric layer have shown many encouraging achievements, including thermal stability[14], output current density[15], output power density[16,17], and cut-off frequency[18], suitable for practical applications.

However, the reported maximum on/off ratio for diamond-based devices still remains in the order of 10^{10}; one of the reasons behind this is that the lower limit of leakage current is in the order of 10^{-8} mA/mm[19,20]. Moreover, the on/off ratio does not exceed 1×10^7 at a temperature of 200°C[14,21], which greatly limits the application of diamond-based devices at high temperature. In addition, when devices are exposed to off-state bias with a relatively high lateral electrical field, it may facilitate the generation of defects or the occurrence of trapping effects[22,23], thereby further increasing the R_{ON} and leakage currents that decreases the on/off ratio.

Herein, a C–H diamond MISFET with a 40-/100-nm Al_2O_3/HfO_2 stacked passivation layer are proposed to achieve a high on/off ratio. A record-setting on/off ratio of $\sim 1 \times 10^{11}$ was achieved, with low $I_{D_leakage}$ and $I_{G_leakage}$ in the order of 10^{-9} mA/mm under off-state conditions at room temperature. Furthermore, a record on/off ratio of $\sim 5 \times 10^9$ was achieved at an ambient temperature of 200°C. The electrical characteristics of the C–H diamond MISFETs under off-state conditions were characterized and analyzed. The off-state leakage current characteristics were monitored by time-dependent leakage current measurements. Further, the information on the trapping effects was characterized using pulsed measurements. Finally, the kinetic properties of the traps and their energy level information were obtained using transient R_{ON} measurements.

Direct-current I–V characteristics

Figs. 1a,b show the cross-sectional schematic and optical microscopic image of the fabricated C–H diamond MISFET. The details of the device fabrication process are provided in the Methods section and Supplementary Fig. 1. The preliminary direct current drain-current–drain-voltage ($I_D - V_{DS}$) characteristics at room temperature are shown in Fig. 1c. The maximum drain current density (I_{D_max}) and R_{ON} were −348 mA/mm, 42.8 Ω·mm, respectively, which are superior to previously reported works with high on/off ratio of $\sim 10^{10}$ (refs. [19,20]). The preliminary direct current gate-voltage (V_{GS}) dependence of I_D, gate-current (I_G), and transconductance (g_m) characteristics at room temperature are shown in Fig. 1d. The threshold voltage (V_{TH}) and maximum g_m were 10.2 V and 32 mS/mm, respectively. The $I_{D_leakage}$ and $I_{G_leakage}$ values were in the order of 10^{-9} mA/mm under off-state conditions, which are lower than that of previous

studies. Benefiting from such low leakage current, an on/off ratio of ~1×10^{11} was achieved in the C–H diamond MISFET, which is the highest value among those of the reported diamond-based devices (Fig. 1e). There are three main reasons for the low leakage current. First, the 40-/100-nm high-k Al_2O_3/HfO_2 introduced fringing capacitances that was conducive to extending the depletion region under off-state conditions, thereby suppressing $I_{D_leakage}$. Second, the Al_2O_3/HfO_2 stacked layer reduced the electric field at the drain edge of the gate[37], causing a reduction in the field-induced leakage current. Third, the good device isolation as well as the relatively-high-quality diamond substrate and dielectric layer.

Although Ren et al. reported an on/off ratio in the order of 10^{10}, after the on/off ratio reached its maximum value, the $I_{D_leakage}$ increased with an increase in gate voltage, resulting in a decreased on/off ratio[19,20]. This may have been due to the increased $I_{G_leakage}$ caused by the increased gate voltage. However, the on/off ratio of the present C–H diamond MISFETs remained roughly constant at the gate voltage swing of ~4 V (Supplementary Fig. 2). The relatively large gate voltage swing under off-state conditions showed that the C–H diamond MISFET was robust to spurious external signals. Nevertheless, the obtained on/off ratio was still lower than that of GaN-based devices (~10^{12})[38]. Furthermore, the subthreshold swing was 0.19 V/dec extracted from the $I_D - V_{GS}$ characteristics; it was comparable to that of reported C–H diamond MISFETs[20,31] but higher than that of GaN-based devices[38]. These results may have been caused by the relatively high interface state density (usually 1×10^{12} $cm^{-2} \cdot eV^{-1}$) in C–H diamond MISFETs[31,39], which limits further improvement in the on/off ratio and subthreshold swing.

High temperature operation is one of the advantages of diamond-based devices. Fig. 2f shows the direct current $I_D - V_{GS}$ characteristics at high temperature conditions. The on/off ratio decreased with the increasing temperature and can be attributed to the effects of high-temperature such as reduced mobility (phonon scattering increase), more severe trapping effects, and increased leakage current. Encouragingly, compared with room temperature, the on/off ratio still remained ~5×10^9 (decreases by only ~20 times) when the temperature is 200°C (Supplementary Fig. 3). This is higher than the previous reported works (Supplementary Table 1), indicating that the C–H diamond MISFETs in this work are capable of operating at high temperature.

Time-dependent off-state leakage characterization

Time-dependent off-state leakage characterization can be used to determine the critical degradation behavior of devices. Here, the leakage currents of the C–H diamond MISFETs were monitored (Methods). When V_{GS} = 14 V, both $I_{D_leakage}$ and $I_{G_leakage}$ barely changed in the V_{DS} range of −10−−22 V (Fig. 2a). However, $I_{D_leakage}$ began to increase with time (~48 s) at V_{DS} = −25 V, whereas $I_{G_leakage}$ did not change significantly. When V_{GS} = 16 V, the leakage currents exhibited a similar trend, whereas the critical breakdown occurred at ~78 s and the magnitude of $I_{D_leakage}$ decreased (Fig. 2b). This implies that a larger gate reverse bias can suppress $I_{D_leakage}$ while also extending the critical breakdown time. Further, the premature breakdown occurred at the Al_2O_3/diamond interface and/or in the diamond substrate

rather than the gate dielectric breakdown. This is mainly due to the generation of defects at the Al_2O_3/diamond interface and/or in the diamond substrate, which is caused by a high electrical field at the drain edge of the gate under off-state conditions with harsher V_{DS}. Therefore, a reduction in the peak of the electrical field at the drain edge of the gate can mitigate the breakdown by using a high-relative-permittivity and thick passivation layer[37].

Pulsed I_D–V_{DS} and I_D–V_{GS} measurements

Pulsed I_D–V_{DS} and I_D–V_{GS} characterizations were employed to eliminate heating effects as much as possible and obtain information on the traps (Methods), which reduce the on/off ratio. The measured pulsed I_D–V_{DS} and I_D–V_{GS} characteristics with a pulse width (PW)/pulse period (PP) = 1 μs/1 ms are shown in Figs. 3a,b. Compared with the quiescent bias condition (V_{GSQ}, V_{DSQ}) = (0 V, 0 V), a negligible change in R_{ON} was observed at (V_{GSQ}, V_{DSQ}) = (14 V, 0 V), whereas a distinct increase in R_{ON} was observed at harsher V_{DSQ}, as shown in Fig. 3a. This implied that the increase in R_{ON} was induced by the trapping effects associated with V_{DSQ}. The first possible explanation is that V_{DSQ} promoted holes to be injected from the gate metal into the stacked passivation layer in the gate–drain access region, i.e., the virtual gate effect[40]. A second possible explanation is that the high electric field between the gate and drain led to the generation of defects at the Al_2O_3/diamond interface and/or in the diamond substrate. Interestingly, as shown in Fig. 3b, there was only a modest change in I_{D_max} between the quiescent bias conditions (0 V, 0 V) and (14 V, 0 V) but a distinct increase in V_{TH} at (14 V, 0 V), compared with (0 V, 0 V). A prominent reduction in I_{D_max} and an increase in V_{TH} were observed under harsh V_{DSQ}. However, the unusual increases in V_{TH} (i.e., the increases in the hole concentration) were contrary to those in previous studies, wherein the trapping effects occurred under the gate region, resulting in a decrease in carrier concentration[22,41,42].

A hole redistribution model was assumed to explain this unusual phenomenon (Fig. 4a). Under off-state conditions, the detrapping effects mainly occurred under the gate region due to the reverse gate quiescent bias V_{GSQ}, thereby increasing the hole concentration and V_{TH}, which is similar to the time-dependent reverse gate bias stress[43]. Simultaneously, the trapping effects mainly happened in the gate–drain access region owing to the gate–drain potential caused by the drain quiescent bias V_{DSQ}, which increased the R_{ON}. In addition, compared with V_{DSQ} = 0 V, a harsher V_{DSQ} led to a larger ΔV_{TH} because a harsher V_{DSQ} increased the potential between the gate and drain, which is equivalent to an increased gate reverse bias, thus causing more prominent detrapping effects.

To verify the proposed hole redistribution model, a series of pulsed I_D–V_{DS} and I_D–V_{GS} characterizations were performed as PP was varied from 100 μs to 10 ms while PW was fixed at 1 μs (Supplementary Fig. 4). The changes in R_{ON} (ΔR_{ON}) and V_{TH} (ΔV_{TH}) at varied PP levels are shown in Figs. 3c,d. It was observed: 1) as PP increased (i.e., stress time increased), ΔR_{ON} and ΔV_{TH} increased, indicating that the variation was time-dependent, following the characteristics of time-dependent bias stress measurements,

2) although the ΔV_{TH} increased, the ΔR_{ON} increased more significantly, particularly under long PP conditions, indicating that the influence of trapping effects on R_{ON} was stronger than that of the detrapping effects, and 3) even if V_{DSQ} = 0 V, the ΔR_{ON} slightly increased with an increase in PP at V_{GSQ} = 14 V; this may be attributed to the generation of the interface state. In particular, more interface states were generated when a harsh V_{DSQ} was applied (Supplementary Section A and Supplementary Fig. 5).

To further investigate the impact of the V_{GSQ} and V_{DSQ} on the ΔR_{ON} and ΔV_{TH}, two sets of pulsed $I_D - V_{DS}$ and $I_D - V_{GS}$ with different quiescent bias conditions (V_{DSQ} = 0 and −16 V when V_{GSQ} is varied) were executed (Supplementary Fig. 6). Fig. 3(e) shows a slight increase in ΔR_{ON} as V_{GSQ} increased at V_{DSQ} = 0 V, whereas ΔR_{ON} significantly increased with increased V_{GSQ} at V_{DSQ} = −16 V. Thus, the increase in R_{ON} was mainly due to the trapping effects caused by V_{DSQ}. Fig. 3(f) shows that ΔV_{TH} increased with an increase in V_{GSQ} in both cases of V_{DSQ} = 0 V and V_{DSQ} = −16 V. The increase in ΔV_{TH} was higher at V_{DSQ} = −16 V than at V_{DSQ} = 0 V. Therefore, a high V_{GSQ} led to more significant detrapping effects under the gate region. In particular, V_{DSQ} enhanced the detrapping effects by increasing the potential between the gate and drain.

R_{ON} transient measurements

To study the kinetic properties of the traps under off-state conditions, transient R_{ON} measurements were performed during off-state stress and corresponding recovery durations (Methods). The change in ΔR_{ON} during the off-state stress (under various drain stress conditions) and the corresponding recovery duration are shown in Fig. 5a. ΔR_{ON} increased with increasing stress duration and $|V_{DS}|$. However, upon removing the corresponding off-state stress conditions for 2 s, ΔR_{ON} increased dramatically. This unusual increase in ΔR_{ON} differed from those obtained in previous studies[22,44,45]. We speculated that ΔR_{ON} increased because the holes were trapped by the gate dielectric layer after removing the off-state stress (Fig. 4b). Transient R_{ON} measurements were conducted at a fixed V_{DS} of −16 V and varied V_{GS}s. As shown in Fig. 5b, ΔR_{ON} increased with increasing stress duration and V_{GS}. Upon removing the corresponding off-state stress condition for 2 s, a distinct increase in ΔR_{ON} was noted, and this increase was linearly related to the increase in V_{GS} (inset, Fig. 5b). These results confirmed that the increase in ΔR_{ON} after removing the off-state stress was predominantly caused by the trapping effects under the gate region.

The properties of the trap levels, which are responsible for the on/off ratio decrease under off-state stress conditions, were investigated via transient R_{ON} measurements at different temperatures. The recovery of R_{ON} after applying (V_{GS}, V_{DS}) = (16 V, −16 V) for 100 s at different temperatures was monitored. Fig. 5c shows the recovery of R_{ON} and its corresponding fitting curve (details of the modified kinetic model used for fitting are provided in Supplementary Section B). A larger ΔR_{ON} and recovery rate were observed when the C–H diamond MISFET was exposed at higher temperatures, indicating that it was thermally activated. The change in R_{ON} can be fitted with stretched exponential kinetics, indicating that the traps had a broad distribution of energy levels[46]. The Arrhenius plot is shown in Fig. 5d; different activation energies (E_{a1} =

0.28 eV and E_{a2} = 0.24 eV) were obtained, which were responsible for the decrease in the on/off ratio. In particular, E_{a1} was primarily related to the trapping effects under the off-state condition that occurred in the gate–drain access region and under the gate region. E_{a2} was mainly associated with the detrapping effects under the off-state condition that occurred under the gate region. The detrapping effects related to the traps with E_{a1} = 0.28 eV had a higher activation energy and a larger time constant than those of the trapping effects related to the traps with E_{a2} = 0.24 eV (under recovery conditions). The relatively large time constant may have been due to the two following main reasons. First, the holes trapped in the traps of the gate dielectric exerted repulsive electrostatic forces on the holes in the stacked passivation layer of the gate–drain access region to hinder the latter from detrapping. Second, the length of the gate–drain access region exceeded the thickness of the gate dielectric layer, thereby increasing the time to detrapping.

Conclusions

C–H diamond MISFETs with a 40-/100-nm Al_2O_3/HfO_2 stacked passivation layer are proposed to reduce the leakage current for low-power-consumption applications. Using a 40-/100-nm Al_2O_3/HfO_2 stacked passivation layer, a prominent reduction in the leakage current was achieved due to the introduction of fringing capacitances and a reduction in the electric field at the drain edge of the gate when compared with previous works. At room temperature, a record-setting on/off ratio of ~1×10^{11} and low current level $I_{D_leakage}$ and $I_{G_leakage}$ in the order of 10^{-9} mA/mm under off-state conditions were realized. A high on/off ratio of ~5×10^9 was still attained at a high temperature of 200°C. These results show the potential of C–H diamond MISFETs proposed in this work for low-power-consumption applications at high temperature.

Using time-dependent off-state leakage measurements, pulsed characterization, and transient R_{ON} measurements, we demonstrated that two types of traps with different activation energies (0.28 and 0.24 eV) can reduce the on/off ratio; furthermore, they can be activated by the electrical field and/or heat. Therefore, improving the growth quality of the dielectric layer and diamond substrate as well as using high-k and thick passivation layer can contribute to reducing the trapping effects and further developing high on/off ratio and high-reliability C–H diamond MISFETs.

Methods

Device fabrication. The (001)-oriented single-crystal chemical vapor deposition (CVD) commercial diamond substrate was used to fabricate the C–H diamond MISFETs. A mixed hot H_2SO_4/HNO_3 solution was used to decontaminate the diamond surface (Supplementary Fig. 1a). The diamond substrate was exposed to hydrogen plasma to generate stable C–H bonds (Supplementary Fig. 1b). The hydrogenation temperature, power, and time were 700°C, 2.2 kW, and 10 min, respectively. After cooling down to room temperature in an H_2 atmosphere, the C–H diamond was placed in the air for several hours to form 2DHG. To form ohmic contacts and protect the 2DHG, a 50-nm-thick Au film was deposited on the C–H diamond surface (Supplementary Fig. 1c). After photolithography and wet etching, the patterns of active

regions were defined. Low-power oxygen plasma was used to isolate the devices because of the high valence-band offset between the C–H and oxygen-terminated diamonds[47] (Supplementary Fig. 1d). After the second photolithography and wet etching, the drain–source spacing was defined at 2.6 μm (Supplementary Fig. 1e). A 40-nm-thick Al_2O_3 film was deposited at 350°C as a gate dielectric and passivation layer using atomic layer deposition (ALD) (Supplementary Fig. 1f). Thereafter, 20-/480-nm Ti/Au was deposited as gate electrodes by electron-beam evaporation on the Al_2O_3 dielectric layer and a lift-off was conducted (Supplementary Fig. 1g). Subsequently, a 100-nm-thick HfO_2 was deposited as the stacked passivation layer by ALD at 300°C (Supplementary Fig. 1h). Finally, another 20-/470-nm Ti/Au metal was deposited to thicken the source and drain electrodes after the oxide windows were opened (Supplementary Fig. 1i). The gate length, gate–drain spacing, and gate–source spacing of the C–H diamond MISFETs were 0.6, 1.5 and 0.5 μm, respectively. By measuring the capacitance–voltage (C–V) characteristics of the metal–insulator–metal (MIM) structures, the relative permittivities of Al_2O_3 and HfO_2 were calculated to be 8.8 and 20.8, respectively.

Measurement setup. Optical microscopy images were obtained using an upright Nikon Eclipse LV100ND metallurgical microscope. The devices under test were placed on a SUMMIT200 probe station with an Unistat 815 thermal control system. The electrical characteristic measurements were conducted using a Keithley 4200A-SCS parameter analyzer. In the case of time-dependent off-state leakage measurements, the total sampling time was ~100 s with a sampling interval of 1 s. The V_{GS} values were 14 and 16 V, respectively. V_{DS} was in the range of −10−−25 V with a step of −3 V. For the pulsed characterizations, the quiescent bias condition (V_{GSQ}, V_{DSQ}) = (0 V, 0 V) was used as a comparison benchmark for other off-state quiescent bias conditions. The gate quiescent bias V_{GSQ} was maintained at 14 V to achieve the off-state conditions, whereas the drain quiescent bias V_{DSQ} was varied from 0 to −22 V. The PW and PP were 1 μs and 1 ms, respectively. In the case of R_{ON} transient measurements, the stress and corresponding recovery durations were set at 100 and 200 s, respectively. During the off-state stress duration, the gate stress was set to 16 V to maintain the off-state condition and various drain stresses were applied. After the stress duration, (V_{GS}, V_{DS}) = (0 V, 0 V) was immediately applied to maintain the C–H diamond MISFET under recovery conditions. A fast (V_{GS}, V_{DS}) = (−2 V, −1 V) measurement was performed to repeatedly interrupt the stress and recovery durations to obtain a dynamic R_{ON}.

Declarations

Data availability

The data that support the findings of this study are available from the corresponding authors on reasonable request. Source data are provided with this paper.

Competing interests

The authors declare no competing interests.

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Figures

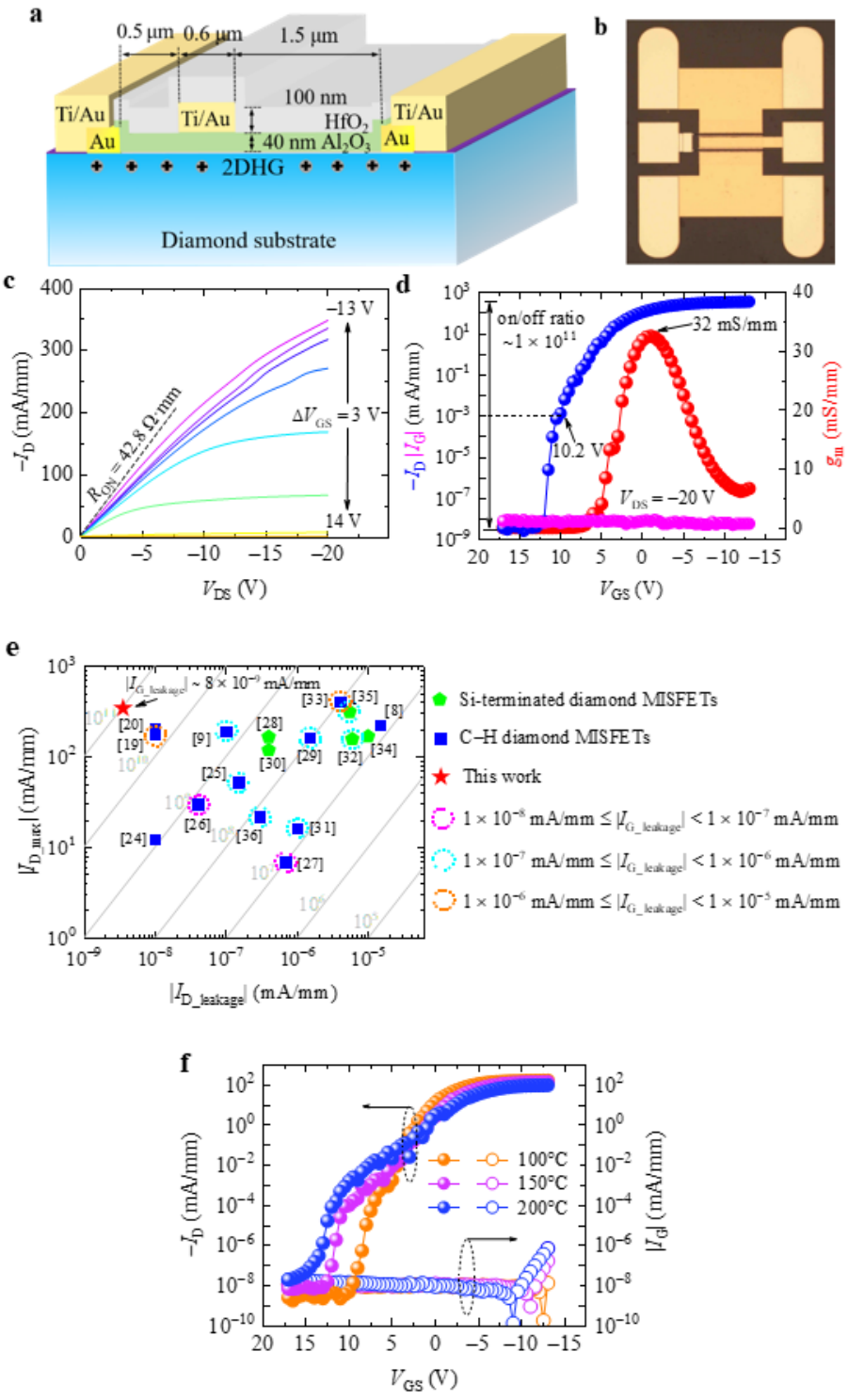


Figure 1

C–H diamond MISFET with a 40-/100-nm Al_2O_3/HfO_2 stacked passivation layer and its electrical characteristics. a,**b**, Cross-sectional schematic (a) and optical microscopy image (b) of the C–H diamond MISFET. **c**,**d**, Direct-current I_D–V_{DS} (c) and I_D–V_{GS} (d) characteristics of the C–H diamond MISFET. Here, the V_{TH} is determined as the gate voltage corresponding to I_{DS} = −1 μA/mm. **e**, Benchmark of $|I_{D_leakage}|$

and $|I_{D_max}|$ of reported C–H diamond MISFETs and Si-terminated diamond MISFETs and those of this study. Additionally, the orders of magnitude of $|I_{G_leakage}|$ of previously reported works are also presented. At present, C–H diamond MISFETs, Si-terminated MISFETs, and doped diamond MISFETs are the common diamond-based FETs with a potential to exhibit high on/off ratios. However, the doped diamond MISFETs have a low output current density and on/off ratio due to their high activation energy; therefore, they are not shown here. **f**, Direct current $I_D - V_{GS}$ and $I_G - V_{GS}$ characteristics of C–H diamond MISFET at various temperature conditions.

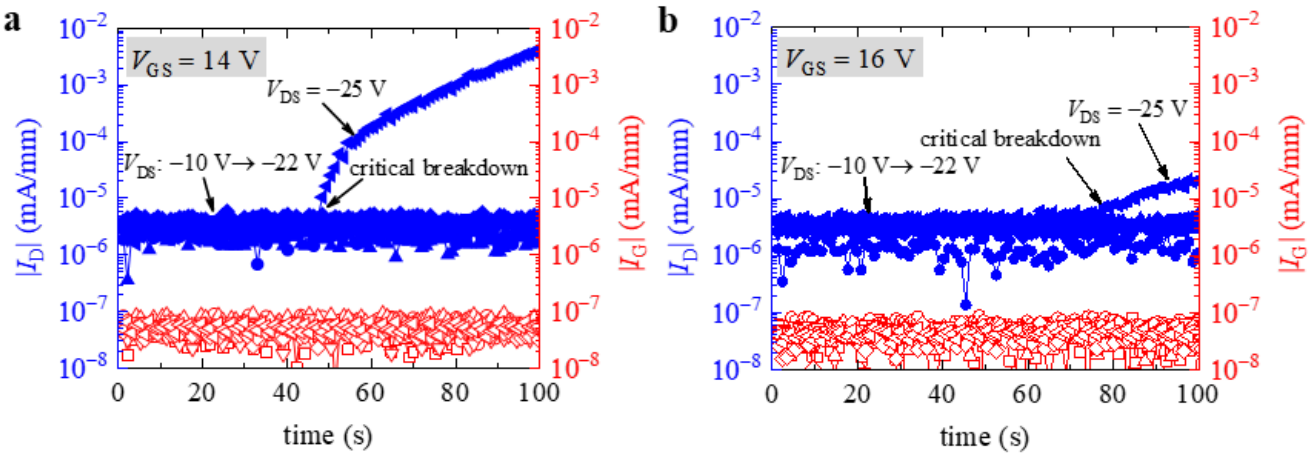


Figure 2

Time-dependent off-state leakage characteristics of C–H diamond MISFETs. **a**, Monitored at V_{GS} = 14 V and different harsh drain biases. **b**, Monitored at V_{GS} = 16 V and different harsh drain biases.

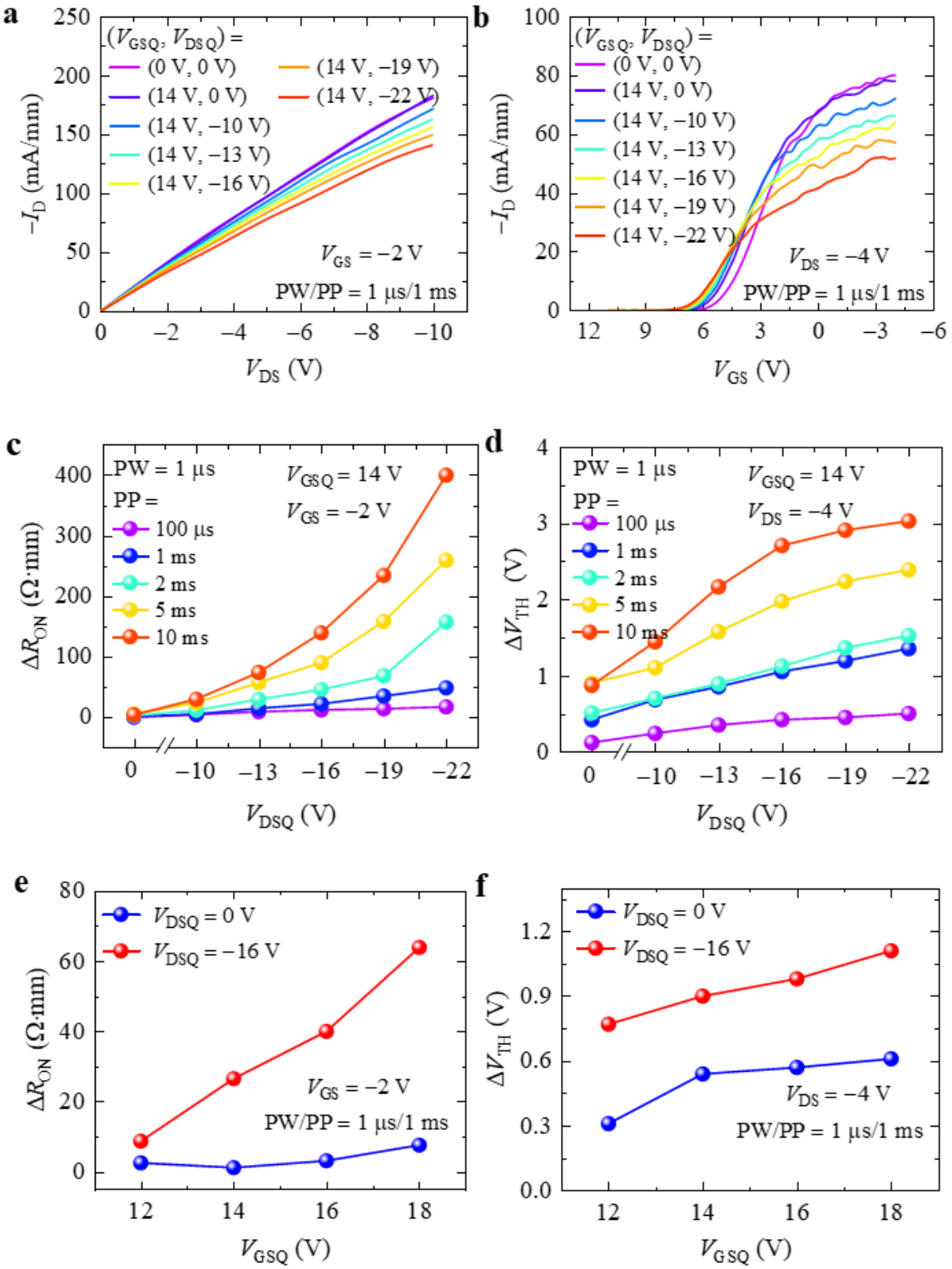


Figure 3

Electrical characteristics of C–H diamond MISFETs by pulsed characterization. a,**b**, Pulsed I_D – V_{DS} (a) and pulsed I_D – V_{GS} (b) characterizations of the C–H diamond MISFET for various quiescent bias conditions under off-state conditions. **c**,**d**, Changes in ΔR_{ON} (c) and ΔV_{TH} (d) under various conditions with PP varied from 100 µs to 10 ms and PW = 1 µs. ΔR_{ON} (ΔV_{TH}) is defined as the R_{ON} (ΔV_{TH}) measured under off-state

quiescent bias conditions minus the R_{ON} (ΔV_{TH}) measured under (V_{GSQ}, V_{DSQ}) = (0 V, 0 V). **e**,**f**, Changes in ΔR_{ON} (e) and ΔV_{TH} (f) under various V_{GSQ} conditions with V_{DSQ} = 0 and −16 V, respectively.

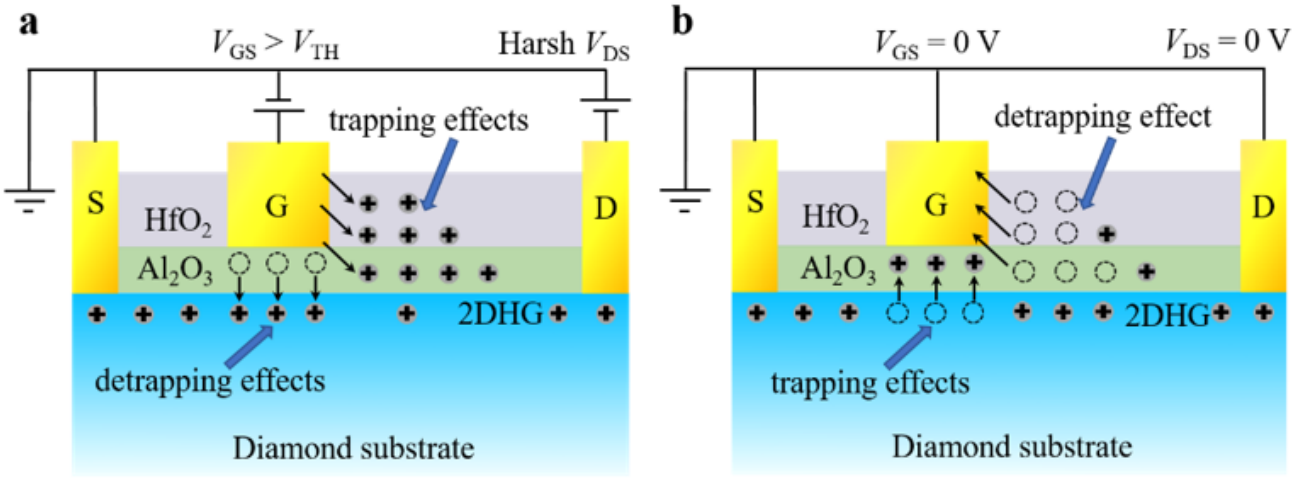


Figure 4

Schematic of the proposed hole redistribution model responsible for the change in V_{TH} and R_{ON} in C–H diamond MISFETs. **a**, Under off-state conditions, the detrapping effects mainly occurred under the gate region owing to the reverse gate bias, increasing the hole concentration and V_{TH}. The trapping effects mainly occurred in the gate–drain access region owing to the gate–drain potential, increasing the R_{ON}. **b**, Under recovery conditions, the trapping effects primarily occurred under the gate region, resulting in a decrease in hole concentration and V_{TH}. The detrapping effects mainly happened in the gate–drain access region, resulting in a decrease in R_{ON}. For brevity, the trapping effects under the gate region under off-state conditions and the detrapping effects under the gate region under recovery conditions are not shown.

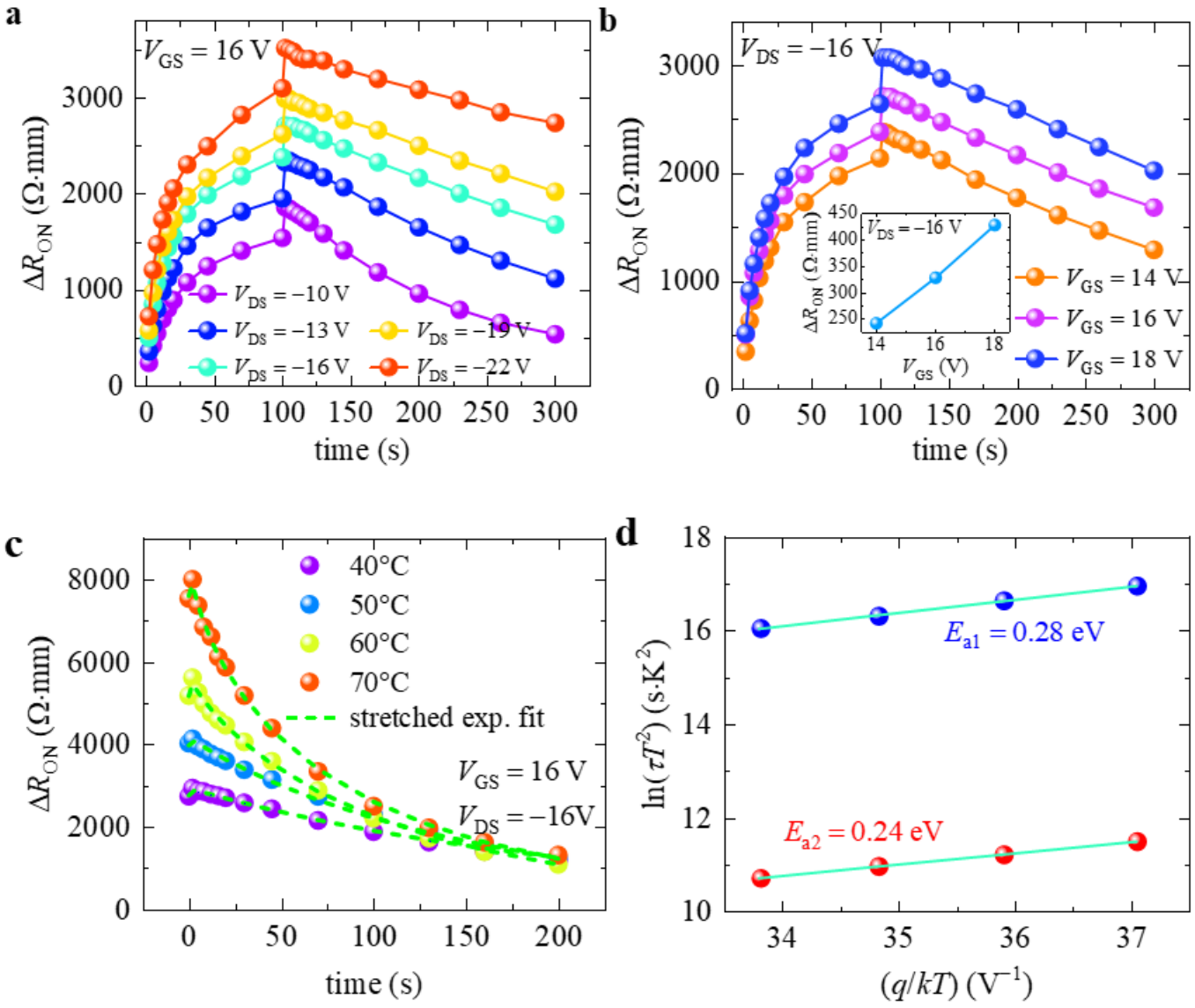


Figure 5

Temperature-dependent electrical characteristics of C–H diamond MISFET. **a**, Changes in ΔR_{ON} during the stress and corresponding recovery durations under various drain stress conditions. The gate bias was 16 V and the drain bias was varied from −10 to − 25 V with a step of −3 V. ΔR_{ON} is defined as the R_{ON} measured during off-state stress and the corresponding recovery duration minus the R_{ON} measured at the initial state. **b**, Changes in ΔR_{ON} during the stress and corresponding recovery durations under various gate stress conditions. The drain bias was −16 V and the gate bias was varied from 14 to 18 V with a step of 2 V. The inset shows the changes in ΔR_{ON} after removing the corresponding off-state stress conditions for 2 s. **c**, Changes in ΔR_{ON} during the recovery duration at different temperatures. **d,** Arrhenius plot.

Supplementary Files

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- 20230318diamondMISFETsupplementarymaterials.pdf