

Pair-wise staggering transmitter for single-ended parallel signaling

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Abstract: A novel pair-wise staggering transmitter is proposed to reduce the crosstalk noise in single-ended channels at high data rates. This work considers two neighboring channels as a pair, and applies staggering between adjacent pairs. As a result, the peak power of crosstalk-induced jitter (CIJ) and glitch (CIG) are reduced by half, so eye becomes larger for a given noise environment, resulting in higher data rate. A prototype IC adopting the proposed approach was fabricated in a 65 nm CMOS process, whose measurement results indicated that the proposed pair-wise 1/2-UI staggering substantially improved the eye height and width at measured operating range of 4.4 to 6.0 Gbps as compared to the conventional 1/2-UI staggering. In terms of maximum data rate, the proposed approach was valid up to over 6 Gbps, whereas the conventional approach was valid merely up to around 4.8 Gbps, indicating 25% improvement.

Keywords: multi-channel, crosstalk, CIJ, CIG, transmitter

Classification: Integrated circuits

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1 Introduction

In a multi-channel environment on a FR4 PCB, the mutual inductance between channels may dominate, resulting in crosstalk due to inductive coupling [1]. The crosstalk noise is expressed as a form of crosstalk-induced jitter (CIJ) or crosstalk-induced glitch (CIG). These types of noise can degrade the channel eye characteristic and may eventually increase channel bit error rate (BER). Various crosstalk cancellation methods have been proposed to solve this problem [2, 3, 4, 5, 6, 7, 8, 9], in which the crosstalk noise cannot be precisely removed even with increased power and area overheads. A data staggering method, which can efficiently suppress the generation of the crosstalk noise using relatively simple hardware, has been proposed [10]. In this method, CIJ can be effectively eliminated, but CIG can never be reduced, resulting in no gain in terms of the worst-case crosstalk noise performance. Hence, BER can still be degraded in a channel configuration where CIG is large. In this paper, a novel pair-wise staggering transmitter (PWS-TX) is presented to effectively reduce the worst-case crosstalk noise power.

2 Proposed pair-wise staggering transmitter

The channel waveforms of the conventional staggering and the proposed pair-wise staggering are shown in Fig. 1(a) and (b), respectively, as exemplified by the 1/2-UI staggering. In each of these figures, since ch2 (ch3) is influenced by the crosstalk caused by ch1 and ch3 (ch2 and ch4), it can be considered as a victim in terms of crosstalk terminology. Ch1 and ch3 (ch2 and ch4) then work as aggressors for the victim. In the signal waveform of the conventional staggering shown in Fig. 1(a), aggressor transitions always occur with 1/2-UI timing difference from victim transitions. With this method, CIJ can be totally eliminated in an ideal situation since the aggressors and the victim have no transitions at the same time. CIG happens without attenuation always at the center of data window, implying that its peak power remains unchanged. As a result, when the crosstalk is large, the amplitude of the CIG will become correspondingly high, resulting in the vertical eye opening greatly reduced and eventually divided into two sections (see 4.4-Gbps and 5.2-Gbps waveforms on the left panels in Fig. 2(c) and (d)). Moreover, when

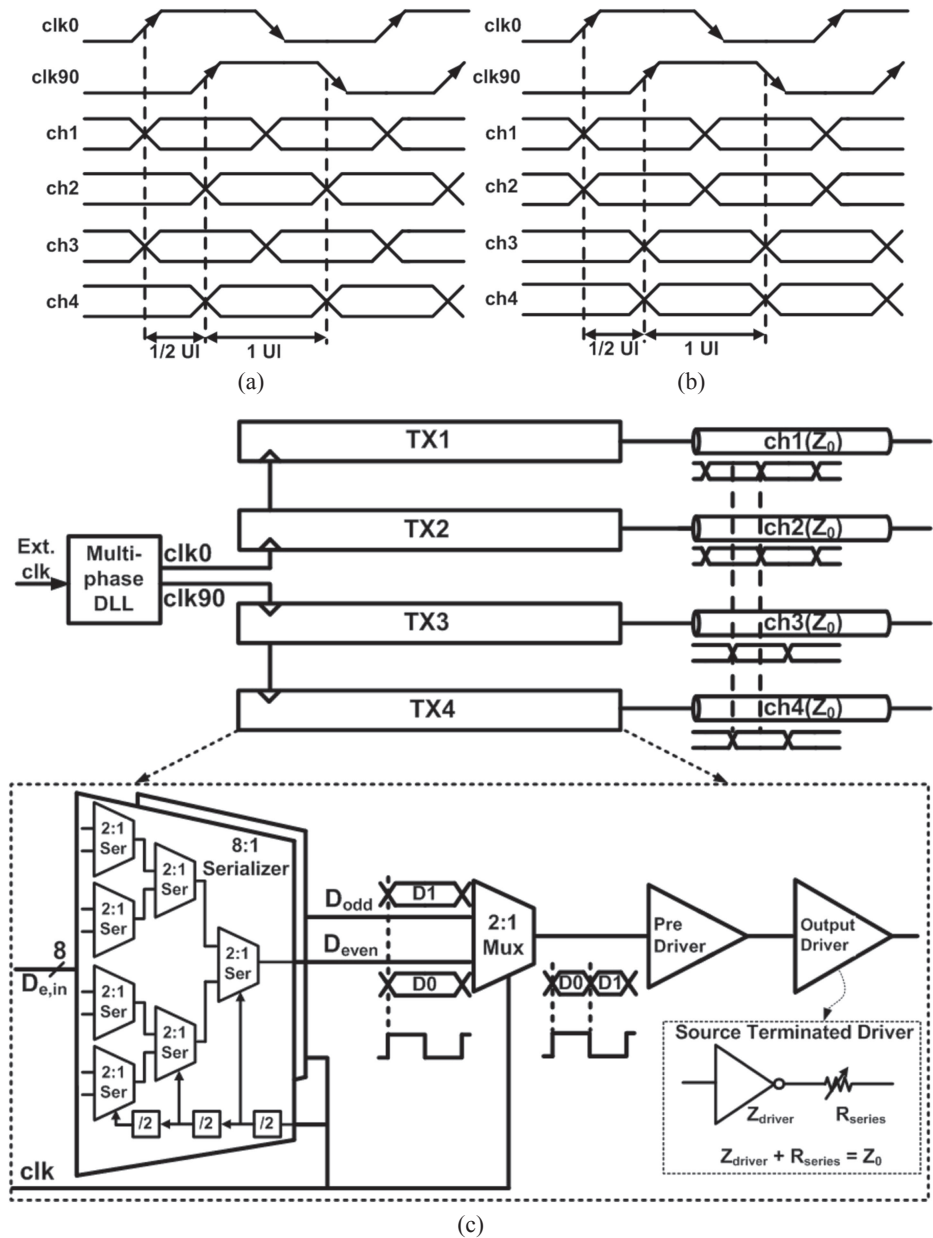


Fig. 1. Timing diagram of (a) conventional staggering, and (b) proposed pair-wise staggering. Block diagram of (c) proposed transmitter with pair-wise 1/2-UI staggering.

the peak power of CIG is large, it may cause undesirable effects on data transition edges, resulting in an increased CIJ and a smaller horizontal eye opening.

To address this issue, a novel pair-wise staggering is proposed as shown in Fig. 1(b), where two neighboring channels are combined as a pair and the staggering is applied between adjacent pairs. With this configuration, the transitions of a victim in a pair occur at the same timing as those of one aggressor in the same pair. The transitions of the other aggressor belonging to the neighboring pair have transitions with 1/2-UI different timing from those of the victim. In Fig. 1(b), ch1 and ch2 belong to a pair, and ch3 and ch4 belong to another pair. So, for a victim of ch2 having ch1 (belonging to the same pair) and ch3 (belonging to the neighboring pair) as aggressors, the victim has the same transition timing as the former and

1/2-UI different transition timing from the latter. For a victim of ch3 where ch2 and ch4 work as aggressors, the victim has the same transition timing as ch4 and 1/2-UI different transition timing from ch2. Using this approach, we'll have an important feature that only one aggressor may cause only one type of crosstalk noise to a victim at any valid timing point. That is, for a victim of ch2, CIJ is caused only by ch1. CIG can be caused by ch1 or ch3 but always at different timing. This feature implies that the peak crosstalk noise power imposed onto a victim channel by neighboring aggressor channels is reduced to a half.

Fig. 1(c) shows the block diagram of a set of transmitters with pair-wise 1/2-UI staggering. In the figure, there are four transmitters, among which two consecutive ones constitute a pair, resulting in two pair configuration. These pairs are driven by two clock phases out of $\pi/2$ phase difference from each other. Transmitters in each pair are driven by an identical clock phase. In Fig. 1(c), since ch1 and ch2 are in one pair and ch3 and ch4 are in another pair, clk0 enters TX1 and TX2, and clk90 enters TX3 and TX4. The required clock phases are generated by a multi-phase delay-locked loop (DLL). Each TX consists of two 8:1 serializers, a 2:1 mux, a pre-driver and a voltage-mode output driver. Each 8:1 serializer has a total of seven 2:1 serializers configured in three stages to generate 1-bit serial data from the incoming 8-bit parallel data. The clock signals used by 2:1 serializers in these stages are with 1/2, 1/4, 1/8 clock frequencies generated by dividing the input clock. Each 2:1 serializer consists of two flip-flops, one latch, and one 2:1 mux. The outputs of two 8:1 serializers, D_{odd} and D_{even} , are transformed into 1-bit data via the 2:1 mux, and pass through the pre-driver and the output driver to reach the channel. The output driver is designed to be a source-terminated configuration, whose output impedance can be externally adjustable to be equal to the characteristic impedance Z_0 of the channel.

3 Measurement results

To assess the performance of the proposed scheme, the conventional 1/2-UI staggering TX and the proposed pair-wise 1/2-UI staggering TX were designed, verified by simulation, and fabricated in a 65 nm CMOS process, whose chip photograph is shown in Fig. 2(a). Fig. 2(b) shows the verification environment having three interconnection channels with package and line parasitics driven by TXs and received by RXs. Unlike Fig. 1(c), a three-channel configuration was designed since one victim with two aggressors is enough to assess the effect of the crosstalk noise. Each channel, whose simulation model consists of segmented resistance (R), self- and mutual-inductance (L_s and L_m), conductance (G), and self- and mutual-capacitance (C_s and C_m), is equally shaped and arranged in parallel with equal spacing. Each physical channel on PCB has a length of 120 mm, a width of 0.65 mm, and a space of 0.09 mm, whose insertion loss is -5 dB at 3 GHz.

Fig. 2(c) and (d) show the simulated and measured eye diagrams at the far end of the victim channel at multiple data rates, respectively. The waveforms on the left belong to the conventional 1/2-UI staggering and those on the right belong to the proposed pair-wise 1/2-UI staggering. For the conventional staggering shown on the left panels in Fig. 2(c) and (d), note that as the data rate increases a large peak

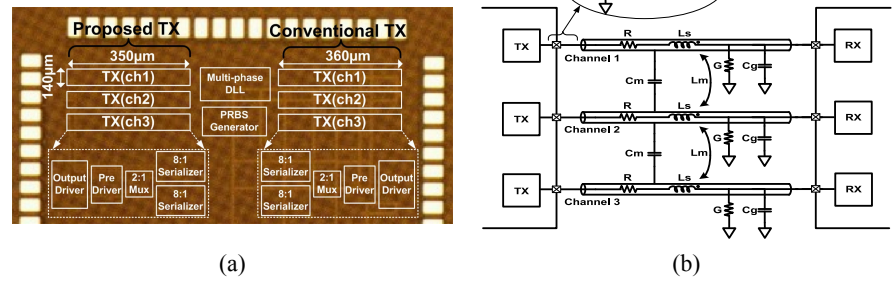
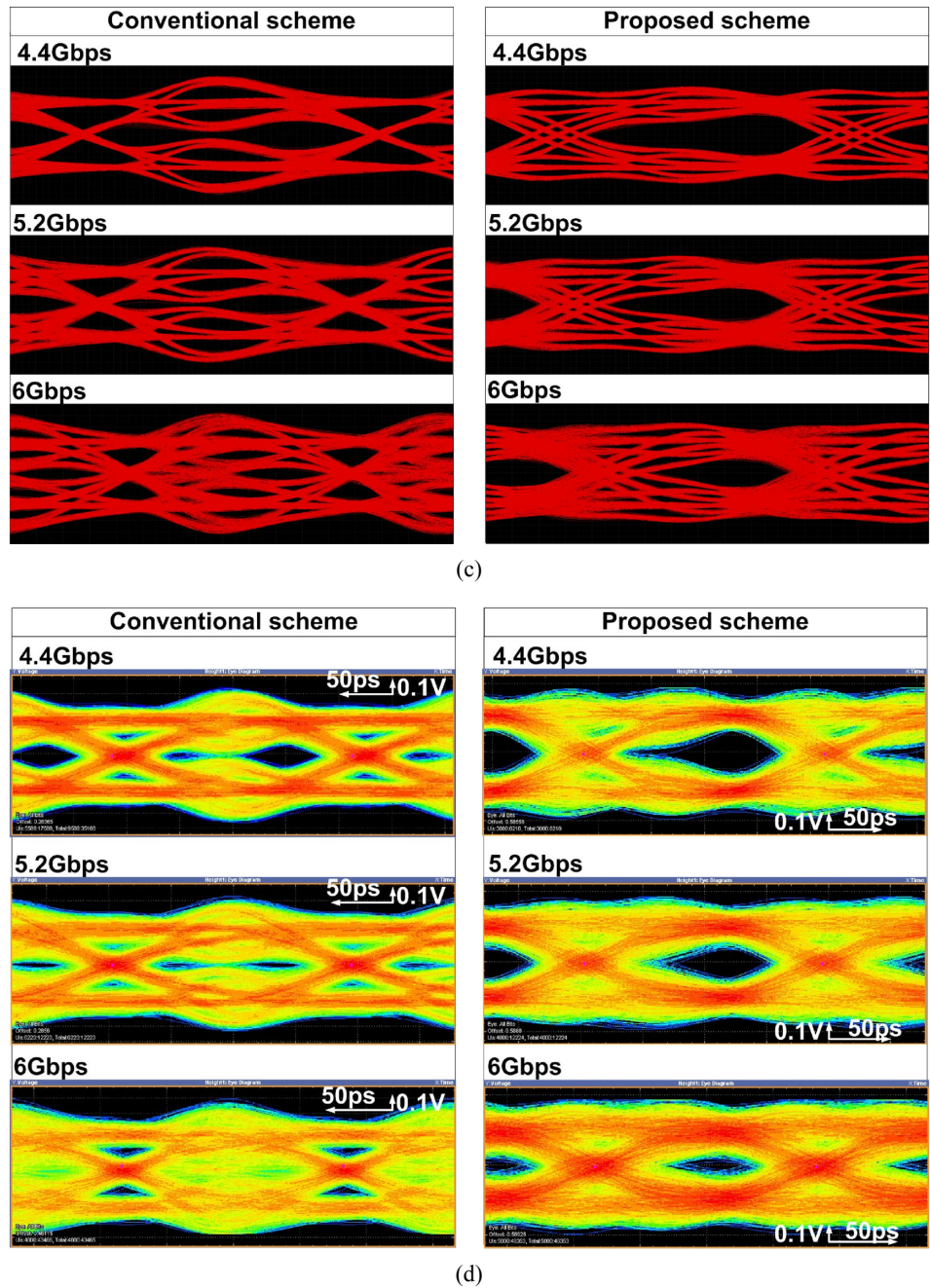


Fig. 2. (a) Chip photograph, (b) channel configuration, (c) simulated eye diagrams, (d) measured eye diagrams.

Table I. Measured performance comparison

		Conventional 1/2-UI staggering	Proposed pair-wise 1/2-UI staggering	Improvement [%]
Peak CIG@2.0 Gbps [V]		0.230	0.120	48
Eye height [V]	@4.4 Gbps	0.116	0.229	97
	@5.2 Gbps	Closed	0.166	
	@6.0 Gbps	Closed	0.050	
Eye width [ns]	@4.4 Gbps	0.058	0.104	79
	@5.2 Gbps	Closed	0.068	
	@6.0 Gbps	Closed	0.041	
Max. data rate [Gbps]		4.8	6.0	25

CIG in the middle tends to divide the eye shape into two sections. So, the eye is getting closed at data rates of above 5.2 Gbps. It is true that the conventional approach apparently allows a smaller CIJ by staggering but due to this undesirable eye bi-section behavior the effect of staggering cannot be fully exploited. This behavior, which is identified by simulated results in Fig. 2(c), is also identically seen in measured results in Fig. 2(d). On the other hand, in the proposed pair-wise 1/2-UI staggering, since the CIG power as well as the CIJ power is reduced to half, a larger eye can be obtained at all data rates considered. That is, since the peak power of CIG is reduced to half, the eye area is not divided. Therefore, the proposed staggering can provide a larger eye and thus a higher data rate, as compared to the conventional staggering. Table I shows the performance comparison between the conventional and proposed staggering schemes, which indicates that the peak CIG voltage is 48% reduced, the eye height and width are 97% and 79% increased, and the maximum data rate is 25% improved.

4 Conclusions

In this paper, a novel pair-wise staggering transmitter is proposed. In a multi-channel environment, two channels are paired and the staggering happens between pairs. Through the test chip fabrication, it was verified that the proposed method is advantageous in removing large crosstalk noise at high data rate.

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